PRM™ and VTM™ Parallel Array Operation

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Contents **Page**

Introduction

VI Chip® PRM Regulators and VTM Current Multipliers can be configured to allow for greater system power capacity. When PRMs and VTMs are connected in an array, the array can support higher current and power than a circuit with a single PRM and VTM. In an array, the PRMs and VTMs must all be of the same type and model number. This note covers Adaptive Loop PRMs (PRM-AL) and the requirements for using them in parallel. A list of applicable PRMs is shown in Table 1.

Part Number	V_{IN} (V)	V_{OUT} (V)	Output Power (W)	Package
MP028x036M12AL	28 (16.1 – 50)	36 (26 – 50)	120	Full Chip
MR028A036M012FP	28 (16.1 – 50)	36 (26 – 50)	120	VI Brick
P024x048T12AL	24 (18 – 36)	48 (26 – 55)	120	Full Chip
PR024A480x012xP	24 (18 – 36)	48 (26 – 55)	120	Full VI Brick
P036x048T12AL	36 (18 – 60)	48 (26 – 55)	120	Full Chip
PR036A480x012xP	36 (18 – 60)	48 (26 – 55)	120	Full VI Brick
P045x048T17AL[1]	45 (38 – 55)	48 (26 – 55)	170	Full Chip
PR045A480x017xP[1]	45 (38 – 55)	48 (26 – 55)	170	Full VI Brick
P045x048T32AL[1]	45 (38 – 55)	48 (26 – 55)	320	Full Chip
PR045A480x032xP[1]	45 (38 – 55)	48 (26 – 55)	320	Full VI Brick
P048x048T12AL[1]	48 (36 – 75)	48 (26 – 55)	120	Full Chip
PR048A480x012xP[1]	48 (36 – 75)	48 (26 – 55)	120	Full VI Brick
P048x048x24AL[1]	48 (36 – 75)	48 (26 – 55)	240	Full Chip
PR048A480x024xP[1]	48 (36 – 75)	48 (26 – 55)	240	Full VI Brick

Table 1
Adaptive Loop PRMs

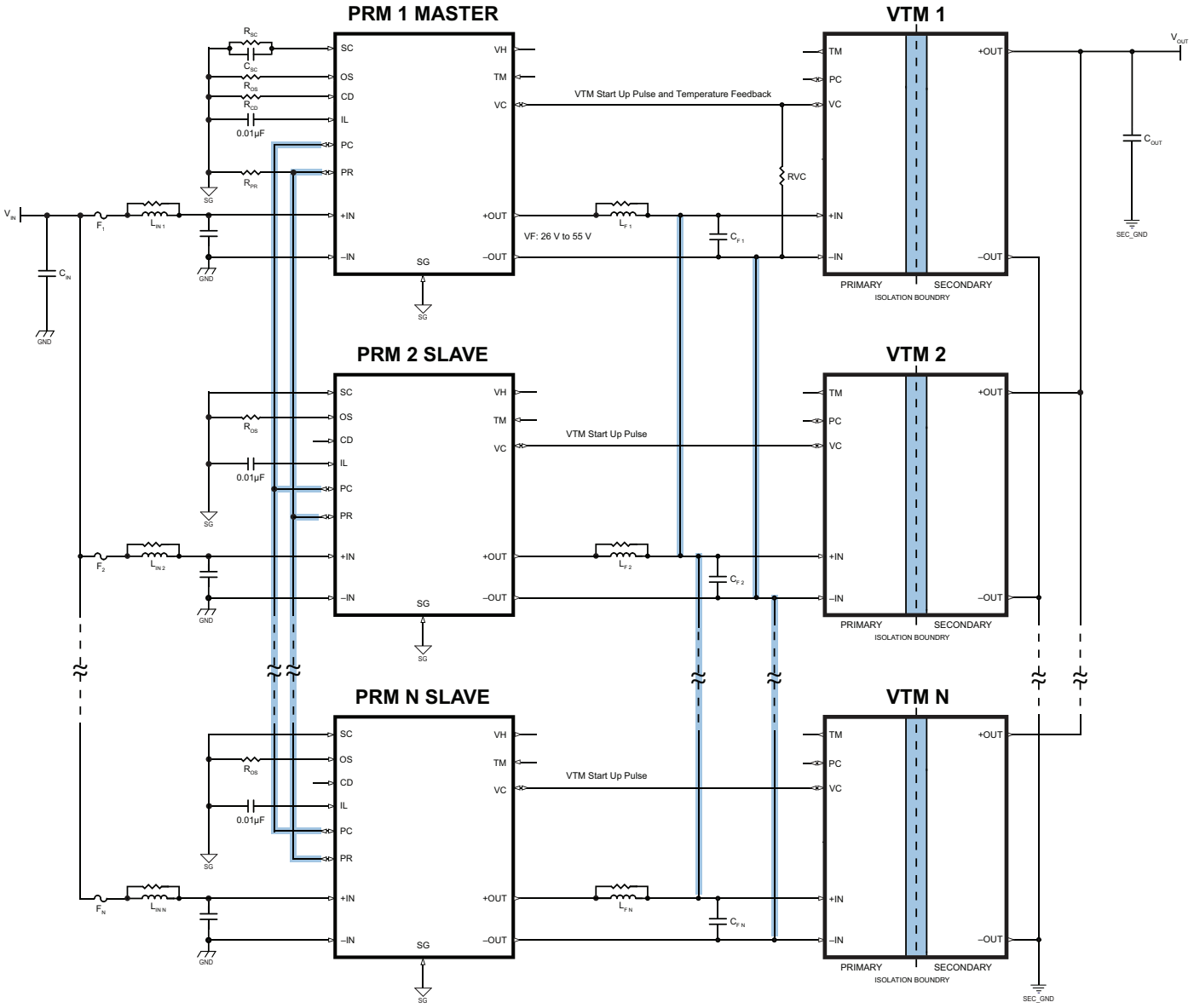
[1] Not recommended for new designs.

High-Level Guidelines

A master-slave configuration is used for arrays of PRMs. Up to five PRMs of the same type may be placed in an array to expand the power capacity of the system. In connecting PRMs in an array, one of the PRMs is designated as the master: it takes control pin inputs and drives the PR bus in an active control loop. Additional PRMs in the array act as slave powertrains only; they use the PR signal as the control input. Referring to the schematic shown in Figure 1, the following guidelines must be considered for the resulting system to start up and operate properly, to avoid overstress on the circuit, and to avoid exceeding the absolute maximum ratings of the components.

- One PRM™ must be designated as a master by configuring the device control pins for intended operation.
- All other PRMs must be designated as slave PRMs by tying SC pins to SG. Vicor recommends making this connection through a 0Ω resistor for troubleshooting purposes.
- All PRMs in the array must have the –IN pins connected together. They must be powered from a common power source, so that the input voltage to each PRM is the same.
- An independent fuse for each PRM +IN connection is required to maintain safety certifications (see Input Fuse Recommendations section of the PRM datasheet).
- An independent inductor for each PRM +IN and +OUT connection is required when used in an array, to control circulating currents among the PRMs and reduce the impact of beat frequencies.
- PRM PC pins must be connected together for startup synchronization. External capacitance on the PC bus is not permitted.
- PR pins must be connected together to enable sharing. The bandwidth requirements of PR are low enough that the bus can be considered a lumped element, rather than a transmission line, and so star connections to the master PRM with stubs, as well as daisy chain connections are permitted.
- A resistor should be connected between master PRMs PR and SG pins in close proximity to the module for noise immunity. The value of the resistor depends on the number of PRMs in the array. Please refer to the Sizing the PR Resistor section for more information.
- The PR trace length between devices should be minimized to avoid introducing additional noise and the PR bus should not be routed under any PRM.
- The SG pin of a PRM is the reference for all control signals internal to the device. The SG pins of all PRMs in the array should connect together to form an SGND reference as shown in Figure 1. If there are significant offsets between –IN connections, series resistors may be needed to prevent excessive current in the SG pins. Refer to the **Layout Considerations** section for more information.
- The VC pin of each PRM in the array must be connected to one or two VC pins of a VTM™, or it must be terminated to –OUT with a 1kΩ resistor. The VC pin must not be left un-terminated for any PRM.
- When operating within an array, the master PRM is rated for full power while the slave PRMs are de-rated to the array rated power and current values provided for slave operation. For PRMs covered in this application note, slaves should be de-rated by 35%. The number of PRMs required to achieve a given array capacity must consider these de-ratings to avoid overstressing any PRM in the array (See Table 2).
- Use of IL trimming within an array is not permitted and all IL pins must be bypassed with a 0.01µF capacitor between the IL and SG pins of each device.
- Slave devices must have a resistor between the OS and SG pins to ensure the maximum OS voltage is not exceeded. Vicor recommends using the same value OS resistor on slaves as the master PRM.
- The Adaptive Loop design procedures will generally hold for any array, although some parameters must adjusted based on the number of PRMs and VTMs in the system.
- All PRMs in the array must be enabled and disabled synchronously. Enabling and disabling PRMs independently within an array (phase shedding) is not permitted.
- Arrays of six or more PRMs may be possible through use of external circuitry. Please refer to **Arrays of Six or More PRMs** to follow.

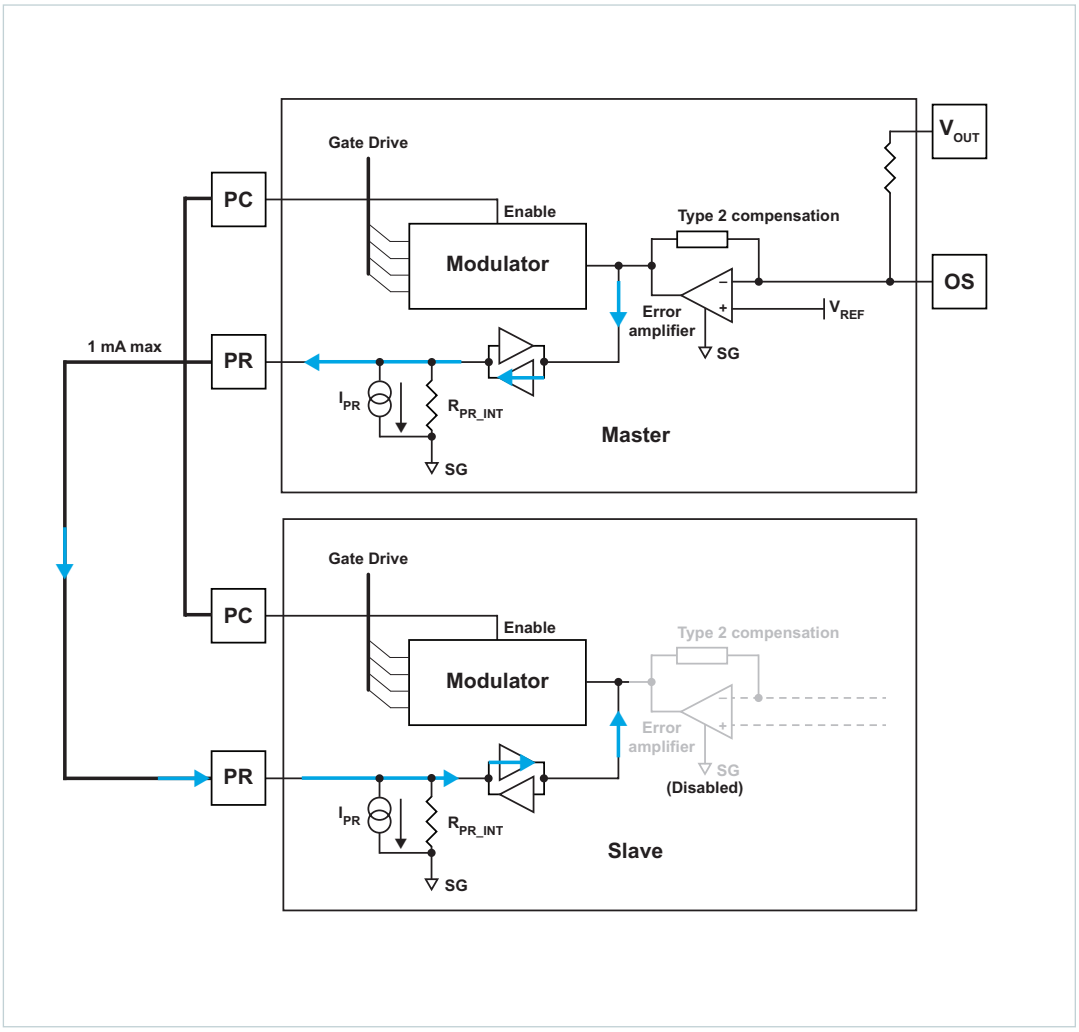
Figure 1
PRM-VTM Parallel Configuration (Up to Five PRMs)



Sizing the PR Resistor

The PR pin of the PRM™ is connected to a bi-directional buffer. The voltage on the controller side of the buffer determines the timing of the power train (and ultimately the power delivered to the load). When designated as a master, an internal error amplifier generates the control signal; the buffer is configured as an output that drives the PR bus. In slave mode, the internal error amplifier is disabled, and the buffer is configured as an input which sinks current. As more slaves are added to the bus, the required drive current from the master increases. The drive capacity of the master will be exceeded with five or more slaves.

Figure 2
PR Current Path from Master to Slave



For noise immunity, an external resistor R_{PR} should be connected between master PRMs PR and SG pins in close proximity to the module. R_{PR} should be sized based on the number of slaves; it should be made as small as possible taking into account the maximum drive current of the master PRM which is limited to 1mA.

Equation 1 and Table 2 show how to calculate the value of the external PR resistor. The internal PR network ($R_{PR\text{-}NT}$ and I_{PR}) sinks a maximum of 250µA and the maximum PR voltage is 7V.

Value of External PR Resistor

$$R_{PR\_EXT} = \frac{7V}{1mA - N_{SLAVES} \bullet (250\mu A)} \qquad (1)$$

Table 2
Calculated Values of PR Resistor

Array Size	Array Rated Power and Current Relative to Data Sheet Rating	N_{SLAVES}	R_{PR_EXT}
2	165%	1	10.0kΩ
3	230%	2	14.0kΩ
4	295%	3	28.0kΩ
5	360%	4	∞ (OPEN)
6	425%	5	External buffer required

Arrays of Six or More PRMs

As mentioned above, the PR pin is specified to drive up to four slaves for a maximum array size of five PRMs. An array of six or more PRMs requires external circuitry.

The recommended circuit is illustrated in Figure 3. An opamp buffer circuit is used in order to limit the loading on the master PR pin. The VH and SG pins of the master PRM™ can be used to supply the opamp provided that the ratings of the VH pin are not exceeded. A 10kΩ resistor should be connected between master PRMs PR and SG pins.

The characteristics of the opamp used for the buffer should be carefully considered. The selected opamp should meet or exceed the specifications of the amplifier internal to the PRM. Table 3 summarizes the key characteristics of the opamp and minimum performance criteria.

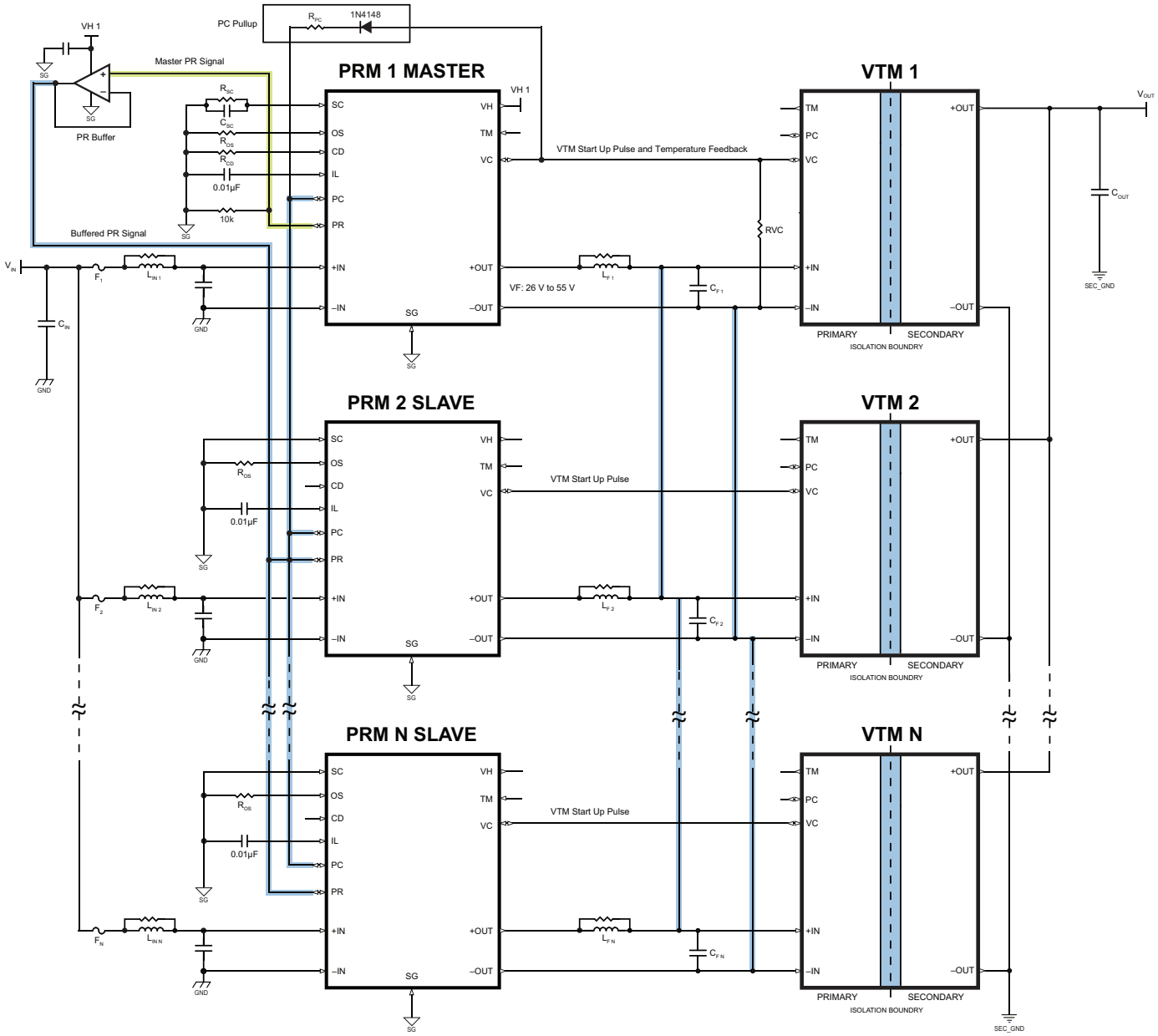
In addition to a PR buffer, the PC bus requires a pull-up to an external source to ensure proper startup. The master PRM VC pin can be used provided the connection is made through a diode. Diode (D1) and pull up resistor (RPC) are illustrated in Figure 3. During normal operation, VC is a control input for the Adaptive Loop circuitry; therefore a low leakage diode such as the 1N4148 must be used to ensure that normal operation and accuracy are not impacted.

Please contact Vicor Applications for assistance with arrays of six or more PRMs.

Table 3
Operational Amplifier Performance Criteria

Parameter	Minimum Requirements	Notes
Supply Current	See Notes	VH is limited to 5mA. The total current draw including opamp supply current must be considered in order to ensure the maximum VH current is not exceeded.
Drive Current	See Notes	Must be capable of driving the PR bus taking into account the current draw of the slave devices.
Bypass Capacitance	≤ 0.1µF	Must be capable of operating with 0.1µF or less to stay within limitations of VH.
Input Offset Voltage	≤ 1mV	Any offsets between the master and slave PR voltages will lead to sharing error. The input offset voltage of the opamp must be minimized.
Slew Rate	≥ 10V/µs	Must be capable of tracking the master PR signal with minimal delay and over/undershoot during transients.
Gain Bandwidth	≥ 10MHz	
Output High Voltage	≥ 7.4V	Should have rail-to-rail output capability and must be capable of driving the PR bus over the full range of 0.4V to 7.4V.
Output Low Voltage	≤ 0.4V	

Figure 3
PRM-VTM Parallel Configuration (Six or More PRMs)



System Considerations

When used with a VTM™, the VC pin provides a pulse of bias power for the VTM during start up. During normal operation, the master PRM™ uses the VC connection for temperature compensation of the adaptive loop (this is done through an internal PTC resistor on the VTM's VC pin). In the slave PRMs, VC is only used for startup; it has no effect on the adaptive loop since slave PRMs use PR as their control input. In general, the VC of each PRM is connected to only one VTM. If necessary, VC can be connected to up to two VTMs, taking into account the resistance of the second VC pin when calculating the loop component values. Circuits with unequal numbers of PRMs and VTMs are discussed in the following section (see AN:024 for more information on adaptive loop settings).

All VTM faults latch the VTM powertrain off. Input power to the system as a whole must be recycled or the PRMs should be disabled and enabled by way of their bussed PC connection in order to restart the system. Vicor recommends that the voltage on the factorized bus be permitted to return to zero before the PRM is re-enabled. Otherwise the soft start of the system may be compromised.

The PC pins of all PRMs in the array should be connected together to synchronize them during startup. The PRM PC pin does not have pull down capability. If a slave PRM faults, the array will continue to operate (with reduced current and power capacity) until the master detects a fault and initiates a restart. Fault synchronization between PRMs and VTMs is possible through the use of external circuitry.

Please contact Vicor Applications Engineering for additional information.

X PRMs to Y VTMs

Whenever possible, each PRM VC should be connected to one VTM VC. Should the number of PRMs be unequal to the number of VTMs, there are certain things to consider during setup. With a greater number of PRMs than VTMs, there will be PRMs left with an un-terminated VC pin. These VC pins must be terminated with a 1kΩ resistor.

In the case that a greater number of VTMs than PRMs are being used, a PRM VC pin can drive up to two VTMs without the need for external circuitry as mentioned above. Connecting an additional VTM to the master VC will impact the adaptive loop settings and temperature compensation since a second PTC resistor is in parallel with the first (see AN:024 for more information on adaptive loop settings).

Driving more than two VTMs requires external circuitry; please contact Vicor Applications Engineering for more details on this configuration.

Figure 4

Two PRM / One VTM Schematic

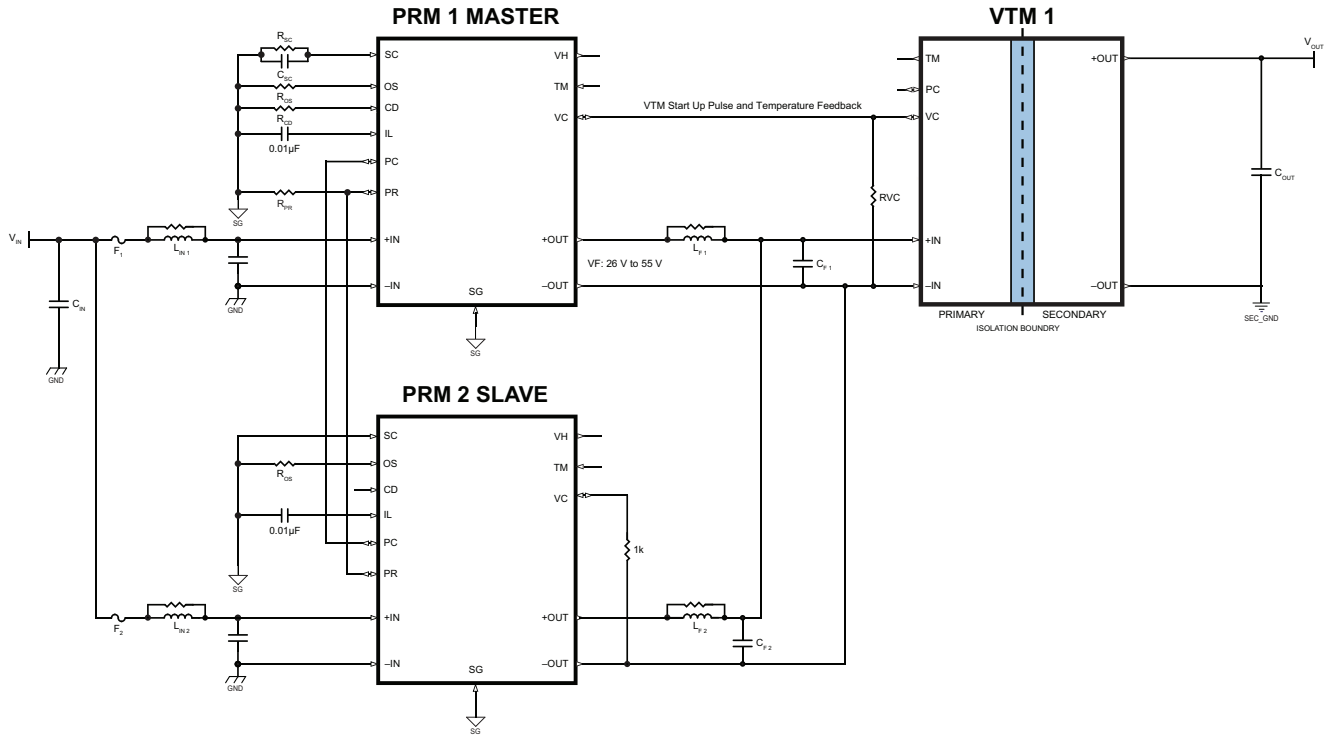
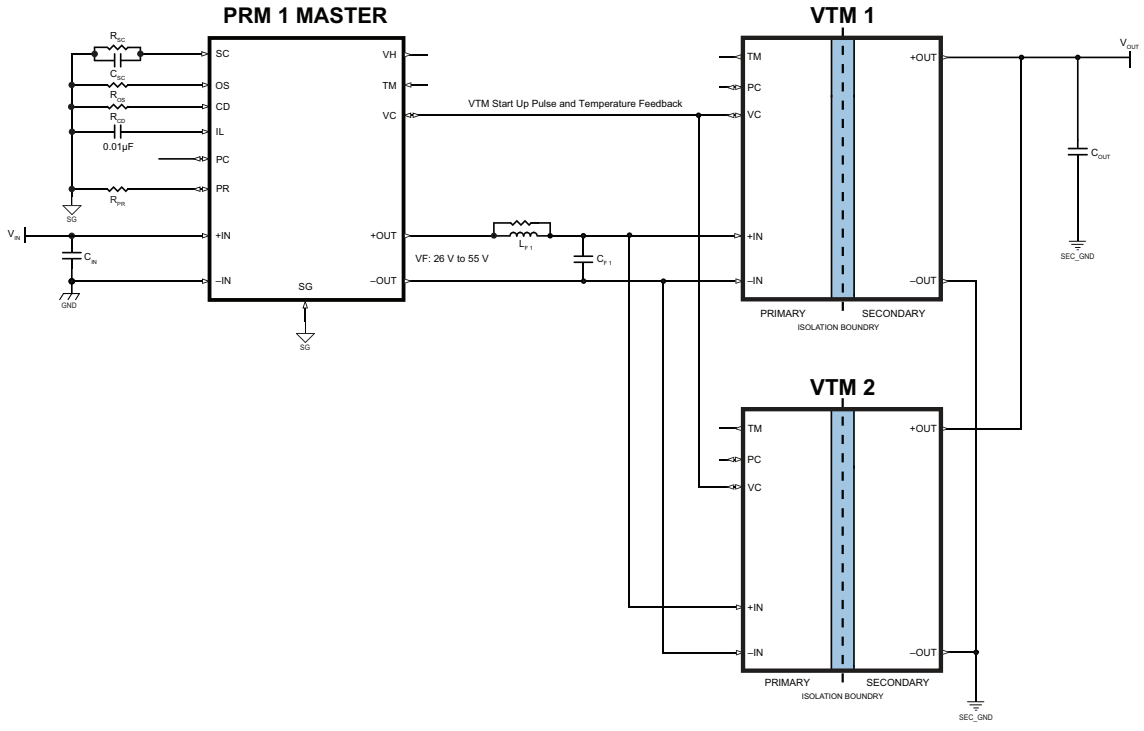


Figure 5

One PRM / Two VTM Schematic



Layout Considerations

Please reference application note AN:005 FPA Printed Circuit Board Layout Guidelines, for a detailed discussion on PCB layout.

Application note AN:005 details board layout recommendations using VI Chip® components, with details on good power connections, reducing EMI, and shielding of control signals and techniques to reference them to SG.

Avoid routing control signals (PC, PR, VC, etc.) directly underneath the PRM™. It is critical that all control signals (aside from VC) are referenced to SG, both for routing and for pull-down and bypassing purposes. VC provides control and feedback from a VTM™, and must be referenced to –OUT of the PRM (–IN of the VTM).

SG connects internally to -IN and is the reference for all control signals within the device. In most applications where PRMs are mounted to the same PCB, the SG pins can be connected together to form an SGND reference node for the array. Current in the SGND reference node should be minimized and SGND should not be tied to any other ground in the system including –IN.

In cases where there is significant resistance between each –IN pin and the common supply return, voltage offsets can be generated between the PRM SG pins, which could cause current flow in the SGND node on the board. Care should be taken to minimize these offsets; otherwise series resistors may be needed between each slave SG pin and the SGND node routed on the board, to ensure the maximum SG current is not exceeded. A slave SG resistor of 1Ω might be typical, but please contact Vicor Applications Engineering for more details.

The PRM senses its output current with an internal shunt connected from –OUT to –IN. In an array, these resistors are in parallel. For best operation, the currents in these sense resistors should be roughly equal, and the return currents among PRMs should be balanced through proper layout. –IN and –OUT cannot be connected together and must be treated as separate nets. Otherwise the internal shunt will be bypassed, disabling current sensing within the device.

Revision History

Revision	Date	Description	Page Number(s)
2.3	04/2014	Updated recommendations and format	All
2.4	04/2014	Updated Figure 4	8

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