

Powering Multiple VTMs with a Single PRM

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Introduction

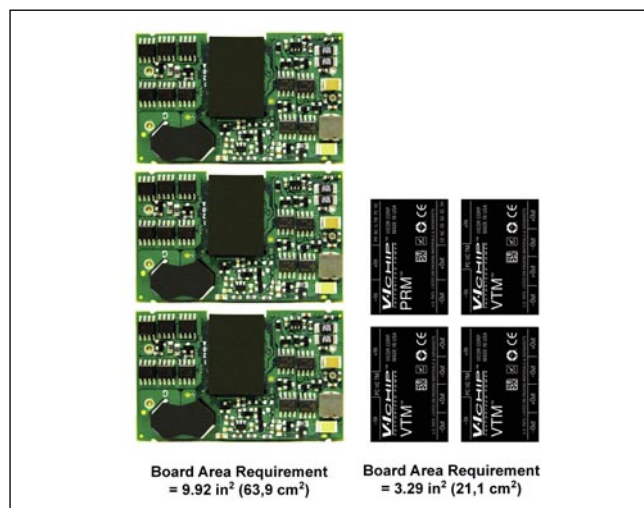
This Application Note discusses the design practices for using V•I Chip PRM Regulators and VTM Current Multipliers to meet the challenge of power systems that require lower voltages, more current, and multiple voltages within one system. Vicor’s V•I Chips can address these challenges.

The two primary building blocks for implementing a V•I Chip solution are the PRMs and VTMs. The PRM provides upstream regulation, while the VTM provides the isolation and voltage transformation at the point of load. In combination, the PRM and VTM enable a complete DC-DC power system with high density, flexibility, and efficiency. For further information regarding the various methods of configuring a power solution using V•I Chips, please use the following link to read our Factorized Power Architecture (FPA) Overview.

www.vicorpower.com/fpa101/fpa101.pdf

For applications that require very accurate output regulation (<1%), a single VTM should be used with one PRM. However, there are many applications that do not require this level of regulation. In cases like these, the PRM can be locally sensed to provide a constant source voltage for multiple VTMs. The regulation of these VTMs will be based on the droop voltage caused by the series impedance of the VTM multiplied by their output current. The regulation for this configuration is typical $\pm 2.5\%$. This solution eliminates duplicate regulation stages, while maintaining individual isolation between the output voltages. For a triple output solution using a standard quarter brick, one brick would be required per output. A V•I Chip solution would require only one PRM and three VTMs. Fig. 1 shows the dramatic decrease in printed circuit board space requirement that can be realized by using V•I Chips.

Figure 1
Brick vs. VIC comparison
(drawn to scale)



The VTM Control (VC) port of the PRM is multiplexed to provide initial start up Vcc voltage to the downstream VTM as well as to receive feedback information from the VTM to compensate for its output impedance.

Fig. 2 shows the typical start up waveforms of a PRM. At start up, before producing an output voltage, the PRM provides initial Vcc to the VTM in the form of a VC pulse. The VC pulse is typically 14 V and lasts between 9 – 15 ms. Approximately 1 – 2 ms after the PRM applies a VC voltage to the VTM, the PRM ramps its output voltage up to its set-point voltage. The VTM will, by receiving VC voltage prior to its input source voltage, synchronize its output voltage rise with its input. The VC voltage can be removed only after the input source exceeds the VTM's input undervoltage lockout. At the end of the VC pulse, the PRM's VC port will start to receive feedback information from the VTM. This reflects the V.I Chip's unique Adaptive Loop regulation technique. The VTM will continue to process power until the input voltage drops below its operating low line voltage or a fault condition occurs. VC voltage must be reapplied in order to restart the VTM.

Figure 2
PRM input versus
output and VC

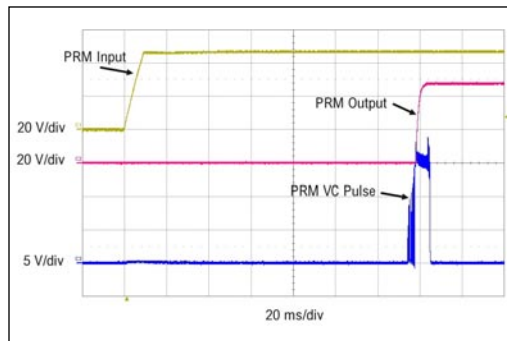


Figure 3
VC Jumpstart voltage and
current waveforms

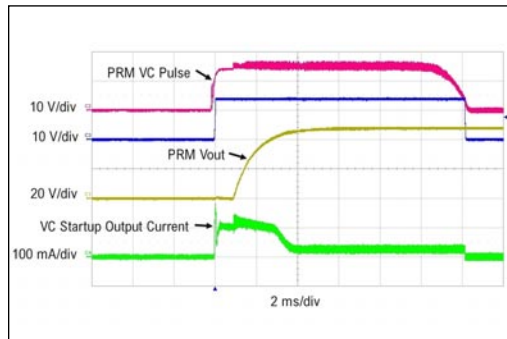
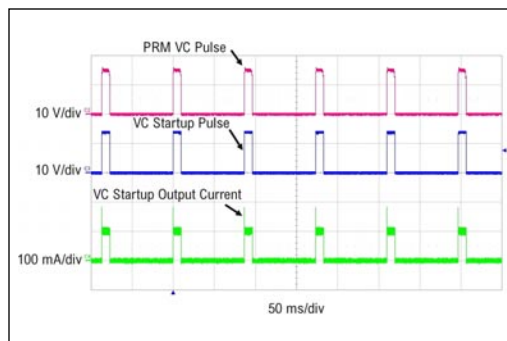


Figure 4
PRM VC and VC Jumpstart
during fault mode



Theory of Operation

On start up, Q2 is used to hold the series pass FET (Q3) off until the PRM issues a VC pulse. When the PRM initiates a VC pulse, Q1 is used to synchronize Q3 so that it replicates the VC pulse width.

The collector of Q4 is clamped to 15 V by D2, which in turn limits the output of the VC Jumpstart circuit to 15 V. R7 is the current sense resistor. Because each VTM may require up to 150 mA at 15 V, the current limit for this example was set for approximately 200 mA. If you intend on starting up more than one VTM from this circuit you will need to increase the current limit as well as review the power dissipation of Q3 so that you do not exceed the FET’s maximum junction temperature. Fig. 3 shows the VC jumpstart voltage and output current waveforms versus the PRM’s VC pulse and output voltage. During a fault condition, such as an over voltage condition on the input to the PRM, the PRM will go into a “hiccup” protection mode and will cycle pulse its VC port. As shown in Fig. 4, the series pass circuit will mirror the VC signal from the PRM to ensure that the additional VTM will properly recover from the fault condition.

Conclusion

This Application Note demonstrates how the addition of a simple series pass circuit extends the PRM’s capability to power more than two VTMs and meets the challenge of power systems that require high current, and multiple voltages within one system. This approach eliminates duplicate converter functions and further reduces both cost, and PC board area.

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Figure 5
Series pass VC start-up circuit

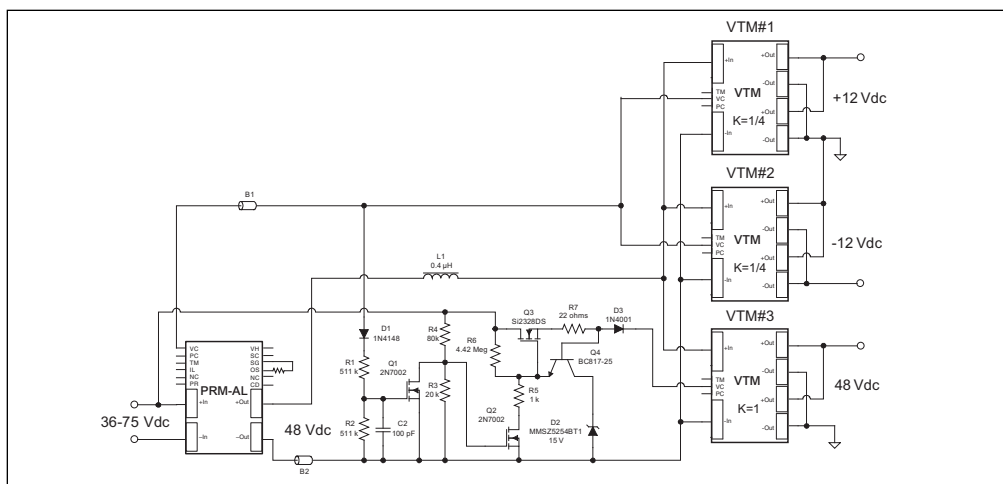


Table 1
Bill of material

Circuit Reference Designator	Part Number	Description & Notes
Ros		Resistor, 2.37 k (1/8 W)
R1		Resistor, 511 k (1/8 W)
R2		Resistor, 511 k (1/8 W)
R3		Resistor, 20.0 k (1/8 W)
R4		Resistor, 80.6 k (1/8 W)
R5		Resistor, 1.00 k (1/8 W)
R6		Resistor, 4.42 M (1/8 W)
R7		Resistor, 22 (1/4 W)
D1	BAS16	High Speed Diode
D2	MMS25254BT1	15 V Zener Diode
D3	S1A	50 V, 1 A General Purpose Rectifier
B1	BLM31PG330SN1L	33 ohm Chip EMIFIL Inductor
B2	BLM31PG330SN1L	33 ohm Chip EMIFIL Inductor
L1	SLC7530D-101ML	SMT inductor, 0.4 μH (Coilcraft)
Q1	2N7002	60 V N-Channel Enhancement Mode FET
Q2	2N7002	60 V N-Channel Enhancement Mode FET
Q3	Si2328DS	100 V N-Channel MOSFET (Siliconix)
Q4	BC817-25	45 V, 500 mA NPN Transistor (Philips)