End of Life - Replaced by VTM48Ex060y040A00

VTM® Current Multiplier
V048F060T040
V048F060M040

High Efficiency, Sine Amplitude Converter™

- 48 V to 6 V VI Chip® Converter
- 40 A (60.0 A for 1 ms)
- High density – 813 W/in³
- Small footprint – 210 W/in²
- Low weight – 0.5 oz (15 g)
- Pick & Place / SMD or Through hole
- 125°C operation (Tj)
- 1 µs transient response
- 3.5 million hours MTBF
- Typical efficiency 95%
- No output filtering required

Product Description
The V048F060T040 VI Chip® current multiplier excels at speed, density and efficiency to meet the demands of advanced power applications while providing isolation from input to output. It achieves a response time of less than 1 µs and delivers up to 40 A in a volume of less than 0.295 in³ with unprecedented efficiency. It may be paralleled to deliver higher power levels at an output voltage settable from 3.25 to 6.87 Vdc.

The VTM V048F060T040's nominal output voltage is 6 Vdc from a 48 Vdc input Factorized Bus, \( V_F \), and is controllable from 3.25 to 6.87 Vdc at no load, and from 2.93 to 6.58 Vdc at full load, over a \( V_F \) input range of 26 to 55 Vdc. It can be operated either open- or closed-loop depending on the output regulation needs of the application. Operating open-loop, the output voltage tracks its \( V_F \) input voltage with a transformation ratio, \( K = \frac{1}{8} \), for applications requiring an isolated output voltage with high efficiency. Closing the loop back to an input PRM® regulator or DC-DC converter enables tight load regulation.

The 6 V VTM module achieves a power density of 813 W/in³ in a VI Chip package compatible with standard pick-and-place and surface mount assembly processes. The VTM modules fast dynamic response and low noise eliminate the need for bulk capacitance at the load, substantially increasing system density while improving reliability and decreasing cost.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Values</th>
<th>Unit</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>+In to -In</td>
<td>-1.0 to 60</td>
<td>Vdc</td>
<td>For 100 ms</td>
</tr>
<tr>
<td>PC to -In</td>
<td>-0.3 to 7.0</td>
<td>Vdc</td>
<td></td>
</tr>
<tr>
<td>VC to -In</td>
<td>-0.3 to 19.0</td>
<td>Vdc</td>
<td></td>
</tr>
<tr>
<td>+Out to -Out</td>
<td>-0.5 to 12</td>
<td>Vdc</td>
<td>Input to output</td>
</tr>
<tr>
<td>Isolation voltage</td>
<td>2,250</td>
<td>Vdc</td>
<td></td>
</tr>
<tr>
<td>Output current</td>
<td>40</td>
<td>A</td>
<td>Continuous</td>
</tr>
<tr>
<td>Peak output current</td>
<td>60.0</td>
<td>A</td>
<td>For 1 ms</td>
</tr>
<tr>
<td>Output power</td>
<td>263</td>
<td>W</td>
<td>Continuous</td>
</tr>
<tr>
<td>Peak output power</td>
<td>395</td>
<td>W</td>
<td>For 1 ms</td>
</tr>
<tr>
<td>Case temperature during reflow[^a]</td>
<td>225</td>
<td>°C</td>
<td>MSL 5</td>
</tr>
<tr>
<td>Operating junction temperature[^b]</td>
<td>-55 to 125</td>
<td>°C</td>
<td>T-Grade</td>
</tr>
<tr>
<td>Storage temperature</td>
<td>-65 to 125</td>
<td>°C</td>
<td>M-Grade</td>
</tr>
</tbody>
</table>

Notes:
[^a]: 245°C reflow capability applies to product with manufacturing date code 1001 and greater.
[^b]: The referenced junction is defined as the semiconductor having the highest temperature. This temperature is monitored by a shutdown comparator.

Part Numbering

- **V**
  - VTM Module
  - Input Voltage Designator

- **048**
  - Output Voltage Designator (\( =V_{OUT} x 10 \))

- **F**
  - Configuration
    - F = J-lead
    - T = Through hole

- **060**
  - Product Grade Temperatures (°C)
    - Storage: Operating (Tj)
      - T: -40 to 125
      - M: -65 to 125
    - Grade: -55 to 125

- **T**
  - Output Current Designator (\( =I_{OUT} \))

- **040**
  - MSL: 5
  - TOB: 4 hrs
### Specifications

#### Input Specs
(Conditions are at 48 \( V_{IN} \), full load, and 25°C ambient unless otherwise specified)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Input voltage range</strong></td>
<td>26</td>
<td>48</td>
<td>55</td>
<td>Vdc</td>
<td>Max Vin = 53 V, operating from -55°C to -40°C</td>
</tr>
<tr>
<td><strong>Input dV/dt</strong></td>
<td>1</td>
<td>V/µs</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Input overvoltage turn on</strong></td>
<td>55.0</td>
<td>Vdc</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Input overvoltage turn off</strong></td>
<td>59.7</td>
<td>Vdc</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Input current</strong></td>
<td>5.5</td>
<td>Adc</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Input reflected ripple current</strong></td>
<td>275</td>
<td>mA</td>
<td>p-p</td>
<td></td>
<td>Using test circuit in Figure 15; See Figure 1</td>
</tr>
<tr>
<td><strong>No load power dissipation</strong></td>
<td>2.0</td>
<td>2.70</td>
<td>W</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Internal input capacitance</strong></td>
<td>1.9</td>
<td>µF</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Internal input inductance</strong></td>
<td>5</td>
<td>nH</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#### Output Specs
(Conditions are at 48 \( V_{IN} \), full load, and 25°C ambient unless otherwise specified)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Output voltage</strong></td>
<td>3.25</td>
<td>6.87</td>
<td>Vdc</td>
<td></td>
<td>No load</td>
</tr>
<tr>
<td><strong>Rated DC current</strong></td>
<td>0</td>
<td>40</td>
<td>Adc</td>
<td>26 - 55 ( V_{IN} )</td>
<td></td>
</tr>
<tr>
<td><strong>Peak repetitive current</strong></td>
<td>60.0</td>
<td>A</td>
<td></td>
<td></td>
<td>Max pulse width 1ms, max duty cycle 10%, baseline power 50%</td>
</tr>
<tr>
<td><strong>Short circuit protection set point</strong></td>
<td>47.4</td>
<td>Adc</td>
<td></td>
<td>Module will shut down</td>
<td></td>
</tr>
<tr>
<td><strong>Current share accuracy</strong></td>
<td>5</td>
<td>10</td>
<td>%</td>
<td>See Parallel Operation on Page 9</td>
<td></td>
</tr>
<tr>
<td><strong>Efficiency</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Half load</td>
<td>94.0</td>
<td>95.6</td>
<td>%</td>
<td>See Figure 3</td>
<td></td>
</tr>
<tr>
<td>Full load</td>
<td>93.5</td>
<td>93.9</td>
<td>%</td>
<td>See Figure 3</td>
<td></td>
</tr>
<tr>
<td><strong>Internal output inductance</strong></td>
<td>1.1</td>
<td>nH</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Internal output capacitance</strong></td>
<td>35.6</td>
<td>µF</td>
<td></td>
<td>Effective value</td>
<td></td>
</tr>
<tr>
<td><strong>Output overvoltage set point</strong></td>
<td>6.9</td>
<td>Vdc</td>
<td></td>
<td>Module will shut down</td>
<td></td>
</tr>
<tr>
<td><strong>Output ripple voltage</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>No external bypass</td>
<td>145</td>
<td>275</td>
<td>mVp-p</td>
<td>See Figures 2 and 5</td>
<td></td>
</tr>
<tr>
<td>10 µF bypass capacitor</td>
<td>13</td>
<td></td>
<td>mVp-p</td>
<td>See Figure 6</td>
<td></td>
</tr>
<tr>
<td><strong>Effective switching frequency</strong></td>
<td>2.1</td>
<td>2.5</td>
<td>3.1</td>
<td>MHz</td>
<td>Fixed, 1.3 MHz per phase</td>
</tr>
<tr>
<td><strong>Line regulation</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( K )</td>
<td>0.1238</td>
<td>1/8</td>
<td>0.1263</td>
<td>( V_{OUT} = K \cdot V_{IN} ) at no load</td>
<td></td>
</tr>
<tr>
<td><strong>Load regulation</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( R_{OUT} )</td>
<td>7.5</td>
<td>8.1</td>
<td>mΩ</td>
<td>See Figure 16</td>
<td></td>
</tr>
<tr>
<td><strong>Transient response</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Voltage overshoot</td>
<td>180</td>
<td>mV</td>
<td></td>
<td>40 A load step with 100 µF ( C_{DC} ); See Figures 7 and 8</td>
<td></td>
</tr>
<tr>
<td>Response time</td>
<td>200</td>
<td>ns</td>
<td></td>
<td>See Figures 7 and 8</td>
<td></td>
</tr>
<tr>
<td>Recovery time</td>
<td>1</td>
<td>µs</td>
<td></td>
<td>See Figures 7 and 8</td>
<td></td>
</tr>
</tbody>
</table>
Specifications

Waveforms

Figure 1 — Input reflected ripple current at full load and 48 V_f.

Figure 2 — Output voltage ripple vs. output current at 48 V_f with no POL bypass capacitance.

Figure 3 — Efficiency vs. output current.

Figure 4 — Power dissipation vs. output current.

Figure 5 — Output voltage ripple at full load and 48 V_f with no POL bypass capacitance.

Figure 6 — Output voltage ripple at full load and 48 V_f with 10 µF ceramic POL bypass capacitance and 20 nH distribution inductance.
Specifications

Parameter | Min | Typ | Max | Unit | Note
--- | --- | --- | --- | --- | ---
Primary Control (PC)
DC voltage | 4.8 | 5.0 | 5.2 | Vdc |  
Module disable voltage | 2.4 | 2.5 | Vdc | VC voltage must be applied when module is enabled using PC
Module enable voltage | 2.5 | 2.6 | Vdc | VC voltage must be applied when module is enabled using PC
Current limit | 2.4 | 2.5 | 2.9 | mA | Source only
Disable delay time | 10 | µs |  | PC low to Vout low
VTM Control (VC)
External boost voltage | 12 | 14 | 19 | Vdc | Required for VTM current multiplier start up without PRM® regulator
External boost duration | 10 | ms |  | Maximum duration of VC pulse = 20 ms

General

- **MTBF**
  - MIL-HDBK-217F
  - 3.5 Mhrs
- **Isolation specifications**
  - Voltage
    - 2,250 Vdc
  - Capacitance
    - 3,000 pF
  - Resistance
    - 10 MΩ
  - Agency approvals
    - CE Marked for Low Voltage Directive and RoHS Recast Directive, as applicable
- **Mechanical**
  - Weight
    - 0.53/15 oz/g
- **Thermal**
  - Over temperature shutdown
    - 125 °C
  - Thermal capacity
    - 9.3 Ws/°C
  - Junction-to-case thermal impedance (RθJC)
    - 1.1 °C/W
  - Junction-to-board thermal impedance (RθJB)
    - 2.1 °C/W

Auxiliary Pins (Conditions are at 48 Vin, full load, and 25°C ambient unless otherwise specified)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>Primary Control (PC)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DC voltage</td>
<td>4.8</td>
<td>5.0</td>
<td>5.2</td>
<td>Vdc</td>
<td></td>
</tr>
</tbody>
</table>
| Module disable voltage | 2.4 | 2.5 | Vdc | VC voltage must be applied when module is enabled using PC
| Module enable voltage | 2.5 | 2.6 | Vdc | VC voltage must be applied when module is enabled using PC
| Current limit | 2.4 | 2.5 | 2.9 | mA | Source only
| Disable delay time | 10 | µs |  | PC low to Vout low
| VTM Control (VC) | | | | | |
| External boost voltage | 12 | 14 | 19 | Vdc | Required for VTM current multiplier start up without PRM® regulator
| External boost duration | 10 | ms |  | Maximum duration of VC pulse = 20 ms

Figure 7 — 0-40 A load step with 100 µF input capacitance and no output capacitance.

Figure 8 — 40-0 A load step with 100 µF input capacitance and no output capacitance.
Pin / Control Functions

+In / -In DC Voltage Ports

The VTM current multiplier input should be connected to the PRM® regulator output terminals. Given that both the regulator and current multiplier have high switching frequencies, it is often good practice to use a series inductor to limit high frequency currents between the PRM module output and VTM module input capacitors. The input voltage should not exceed the maximum specified. If the input voltage exceeds the overvoltage turn-off, the VTM module will shutdown. The VTM module does not have internal input reverse polarity protection. Adding a properly sized diode in series with the positive input or a fused reverse-shunt diode will provide reverse polarity protection.

TM – For Factory Use Only

VC – VTM Control

The VC port is multiplexed. It receives the initial Vcc voltage from an upstream PRM regulator, synchronizing the output rise of the VTM module with the output rise of the regulator. Additionally, the VC port provides feedback to the PRM to compensate for the current multiplier output resistance. In typical applications using VTM modules powered from PRM regulators, the regulators VC port should be connected to the VTM module VC port.

The VC port is not intended to be used to supply Vcc voltage to the VTM module for extended periods of time. If VC is being supplied from a source other than the PRM regulators, the voltage should be removed after 20 ms.

PC – Primary Control

The Primary Control (PC) port is a multifunction port for controlling the current multiplier as follows:

Disable – If PC is left floating, the VTM module output is enabled. To disable the output, the PC port must be pulled lower than 2.4 V, referenced to -In. Optocouplers, open collector transistors or relays can be used to control the PC port. Once disabled, 14 V must be re-applied to the VC port to restart the VTM module.

Primary Auxiliary Supply – The PC port can source up to 2.4 mA at 5 Vdc.

+Out / -Out DC Voltage Output Ports

The output and output return are through two sets of contact locations. The respective +Out and –Out groups must be connected in parallel with as low an interconnect resistance as possible. Within the specified input voltage range, the Level 1 DC behavioral model shown in Figure 16 defines the output voltage of the VTM module. The current source capability of the VTM module is shown in the specification table.

To take full advantage of the VTM current multiplier, the user should note the low output impedance of the device. The low output impedance provides fast transient response without the need for bulk POL capacitance. Limited-life electrolytic capacitors required with conventional converters can be reduced or even eliminated, saving cost and valuable board real estate.
Mechanical Drawings

Figure 10 — VTM module J-Lead mechanical outline; Onboard mounting

Figure 11 — VTM module J-Lead PCB land layout information; Onboard mounting
Mechanical Drawings (continued)

Figure 12 — VTM through-hole module mechanical outline

Figure 13 — VTM through-hole module PCB layout information
RECOMMENDED LAND PATTERN
(NO GROUNDING CLIPS)
TOP SIDE SHOWN

DASHED LINE
INDICATES
VE POSITION

RECOMMENDED LAND PATTERN
(With GROUNDING CLIPS)
TOP SIDE SHOWN

DASHED LINE
INDICATES
VE POSITION

NOTES:
1. MAINTAIN 3.50 [0.138] DIA. KEEP-OUT ZONE FREE OF COPPER, ALL PCB LAYERS.
2. (A) MINIMUM RECOMMENDED PITCH IS 39.50 [1.555], THIS PROVIDES 7.00 [0.275] COMPONENT EDGE-TO-EDGE SPACING, AND 0.50 [0.020] CLEARANCE BETWEEN VICOR HEAT SINKS.
   (B) MINIMUM RECOMMENDED PITCH IS 41.00 [1.614], THIS PROVIDES 8.50 [0.334] COMPONENT EDGE-TO-EDGE SPACING, AND 2.00 [0.079] CLEARANCE BETWEEN VICOR HEAT SINKS.
3. VI CHIP® MODULE LAND PATTERN SHOWN FOR REFERENCE ONLY; ACTUAL LAND PATTERN MAY DIFFER. DIMENSIONS FROM EDGES OF LAND PATTERN TO PUSH-PIN HOLES WILL BE THE SAME FOR ALL FULL SIZE VI CHIP PRODUCTS.
4. RoHS COMPLIANT PER CST-0001 LATEST REVISION.
5. UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE MM [INCH]. TOLERANCES ARE:
   X.X [X.XX] = ±0.3 [0.01]
   X.XX [X.XXX] = ±0.13 [0.005]
6. PLATED THROUGH HOLES FOR GROUNDING CLIPS (33855) SHOWN FOR REFERENCE. HEAT SINK ORIENTATION AND DEVICE PITCH WILL DICTATE FINAL GROUNDING SOLUTION.

Figure 14 — Hole location for push pin heat sink relative to VI Chip® module
**Parallel Operation**

In applications requiring higher current or redundancy, VTM current multipliers can be operated in parallel without adding control circuitry or signal lines. To maximize current sharing accuracy, it is imperative that the source and load impedance on each VTM module in a parallel array be equal. If the modules are being fed by an upstream PRM® regulator, the VC nodes of all VTM modules must be connected to the PRM module VC.

To achieve matched impedances, dedicated power planes within the PC board should be used for the output and output return paths to the array of paralleled VTMs. This technique is preferable to using traces of varying size and length.

The VTM module power train and control architecture allow bi-directional power transfer when the module is operating within its specified ranges. Bi-directional power processing improves transient response in the event of an output load dump. The module may operate in reverse, returning output power back to the input source. It does so efficiently.

**Thermal Considerations**

VI Chip® products are multi-chip modules whose temperature distribution varies greatly for each part number as well as with the input/output conditions, thermal management and environmental conditions. Maintaining the top of the V048F060T040 case to less than 100°C will keep all junctions within the VI Chip module below 125°C for most applications. The percent of total heat dissipated through the top surface versus through the J-lead is entirely dependent on the particular mechanical and thermal environment. The heat dissipated through the top surface is typically 60%. The heat dissipated through the J-lead onto the PCB board surface is typically 40%. Use 100% top surface dissipation when designing for a conservative cooling solution.

It is not recommended to use a VI Chip module for an extended period of time at full load without proper heat sinking.

**Input Impedance Recommendations**

To take full advantage of the current multiplier’s capabilities, the impedance of the source (input source plus the PC board impedance) must be low over a range from DC to 5 MHz. Input bypass capacitance may be added to improve transient performance or compensate for high source impedance. The VTM module has extremely wide bandwidth so the source response to transients is usually the limiting factor in overall output response of the module.

Anomalies in the response of the source will appear at the output of the VTM module, multiplied by its K factor of $\frac{1}{8}$. The DC resistance of the source should be kept as low as possible to minimize voltage deviations on the input to the module. If the module is going to be operating close to the high limit of its input range, make sure input voltage deviations will not trigger the input overvoltage turn-off threshold.

**Input Fuse Recommendations**

VI Chip products are not internally fused in order to provide flexibility in configuring power systems. However, input line fusing of VI Chip modules must always be incorporated within the power system. A fast acting fuse is required to meet safety agency Conditions of Acceptability. The input line fuse should be placed in series with the +In port.

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**Application Note**

**Input reflected ripple measurement point**

- F1 7A Fuse
- C1 47 µF Al electrolytic
- C2 0.47 µF ceramic
- 14 V

**Notes:**
- C3 should be placed close to the load
- R3 may be ESR of C3 or a separate damping resistor.

*Figure 15 — VTM module test circuit*
Application Note (continued)

VTM Current Multiplier Level 1 DC Behavioral Model for 48 V to 6 V, 40 A

Figure 16 — This model characterizes the DC operation of the VI Chip® VTM, including the converter transfer function and its losses. The model enables estimates or simulations of output voltage as a function of input voltage and output load, as well as total converter power dissipation or heat generation.

VI Chip® VTM Current Multiplier Level 2 Transient Behavioral Model for 48 V to 6 V, 40 A

Figure 17 — This model characterizes the AC operation of the VI Chip® VTM including response to output load or input voltage transients or steady state modulations. The model enables estimates or simulations of input and output voltages under transient conditions, including response to a stepped load with or without external filtering elements.

In figures below:

K = VTM current multiplier transformation ratio
RO = VTM output resistance
VF = PRM® output (Factorized Bus Voltage)
VO = VTM output
VL = Desired load voltage

FPA™ Adaptive Loop

Figure 18 — The PRM regulator controls the factorized bus voltage, Vf, in proportion to output current to compensate for the output resistance, Ro, of the VTM current multiplier. The VTM module output voltage is typically within 1% of the desired load voltage (VL) over all line and load conditions.
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