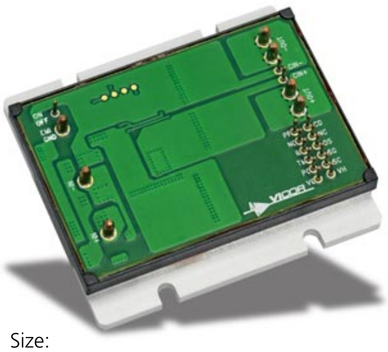
MIL-COTS PRM™ Regulator with Integrated Filter (MR028B036M012FPT)



Size:
2.19 x 1.91 x 0.37 in
53,7 x 48,6 x 9,5 mm

Features

- -55°C to 100°C baseplate operation
- Vin range: 16.5 – 50 Vdc (13.9 – 50 Vdc after startup)
- EMI filtering: MIL-STD-461E/F
- Transient protection MIL-STD-704A/E/F and MIL-STD-1275A/B/D
- High density: up to 78 W/in^3
- Height above board: 0.37 in (9.5 mm)
- Low weight: 2.19 oz (62.1g)
- ZVS buck-boost regulator
- Typical efficiency: 95%
- 1.3 MHz switching frequency
- Low noise operation
- Architectural flexibility

Product Overview

The VI BRICK Pre-Regulator Module with integrated filter is a very efficient non-isolated regulator capable of both boosting and bucking a wide range input voltage. It is specifically designed to provide a controlled Factorized Bus distribution voltage for powering downstream VI BRICK Current Multiplier Modules — fast, efficient, isolated, low noise Point-of-Load (POL) converters. In combination, VI BRICK PRMs and VTMs™ form a complete DC-DC converter subsystem offering all of the unique benefits of Vicor's Factorized Power Architecture (FPA): high density and efficiency; low noise operation; architectural flexibility; extremely fast transient response; and elimination of bulk capacitance at the Point-of-Load (POL). In addition, the integrated filter provides compliance to MIL-STD-1275 and MIL-STD-704 for (transients) and MIL-STD-461 (EMI).

In FPA systems, the POL voltage is the product of the Factorized Bus voltage delivered by the VI BRICK PRM and the "K-factor" (the fixed voltage transformation ratio) of a downstream VTM. The PRM controls the Factorized Bus voltage to provide regulation at the POL. Because VTMs perform true voltage division and current multiplication, the Factorized Bus voltage may be set to a value that is substantially higher than the bus voltages typically found in "intermediate bus" systems, reducing distribution losses and enabling use of narrower distribution bus traces. A Military COTS VI BRICK PRM-VTM chip set can provide up to 100 A or 120 W.

The Military COTS VI BRICK PRM with integrated filter described in this data sheet features a unique "Adaptive Loop" compensation feedback: a single wire alternative to traditional remote sensing and feedback loops that enables precise control of an isolated POL voltage without the need for either a direct connection to the load or for noise sensitive, bandwidth limiting, isolation devices in the feedback path.

Absolute Maximum Ratings

Parameter	Values	Unit	Notes
+In to -In	-1.0 to 60.0	Vdc	Continuous
PC to -In	-0.3 to 6.0	Vdc	
PR to -In	-0.3 to 9.0	Vdc	
IL to -In	-0.3 to 6.0	Vdc	
VC to -In	-0.3 to 18.0	Vdc	
+Out to -Out	-0.3 to 59	Vdc	
SC to -Out	-0.3 to 3.0	Vdc	
VH to -Out	-0.3 to 9.5	Vdc	
OS to -Out	-0.3 to 9.0	Vdc	
CD to -Out	-0.3 to 9.0	Vdc	
SG to -Out	100	mA	
Continuous output current	3.3	Adc	
Continuous output power	120	W	
Operating temperature	-55 to +100	°C	M-Grade; baseplate
Storage temperature	-65 to +125	°C	M-Grade

Note: Stresses in excess of the maximum ratings can cause permanent damage to the device. Operation of the device is not implied at these or any other conditions in excess of those given in the specification. Exposure to absolute maximum ratings can adversely affect device reliability.

SPECIFICATIONS

PART NUMBERING

MR	028	B	036	M	012	F	P	T
Pre-Regulator Module	Input Voltage Designator	Package Size	Nominal Factorized Bus Voltage	Product Grade Temperatures (°C)	Output Power Designator (=P_{OUT} /10)	Baseplate	Pin Style	

Product Grade Temperatures (°C)

Grade	Operating	Storage
M =	-55 to +100	-65 to +125

Baseplate

F = Slotted flange

Pin Style

P = Through hole

Input Specifications *(Conditions are at 28 Vin, 36 Vf [a], full load, and 25°C baseplate unless otherwise specified)*

Parameter	Min	Typ	Max	Unit	Notes
Input voltage range	16.5[b]	28	50	Vdc	
Input dV/dt			1	V/µs	
Input undervoltage turn-on		15.9	16.1	Vdc	Increases linearly to 17 V max at 100°C
Input undervoltage turn-off		13.9		Vdc	
Input overvoltage turn-on	50.5	52.9		Vdc	
Input overvoltage turn-off		53.9	55.4	Vdc	
Input quiescent current		0.5	1	mA	PC low
Input current		4.5		Adc	
Input reflected ripple current		240		mA p-p	See Figures 3
No load power dissipation		2.75	5.8	W	
Internal input capacitance		5		µF	Ceramic
Recommended external capacitance (C_{IN})		1,000		µF	Input filter circuit Figure 12 C_{IN}
Transient Immunity			100	Vdc	50 ms per MIL-STD-1275A/B/D
			250	Vdc	70 µs per MIL-STD-1275A/B/D
			70	Vdc	20 ms per MIL-STD-704A
			80	Vdc	100 ms per D0-160 E, sec.16, Cat. z
			50	Vdc	12.5 ms per Mil-STD-704 E/F

[a] Vf is factorized bus voltage (see Figure 16).
[b] Will operate down to 13.9 V after start up ≥ 16 V.

Output Specifications *(Conditions are at 28 Vin, 36 Vf [a], full load, and 25°C baseplate unless otherwise specified)*

Parameter	Min	Typ	Max	Unit	Note
Output voltage range	26	36	50	Vdc	Factorized Bus voltage (Vf) set by R_{OS}
Output power	0		120	W	
Internal voltage drop		0.4		Vdc	
Output current	0		3.33	Adc	
DC current limit	3.5	3.9	4.4	Adc	I_L pin floating
Average short circuit current		0.125	1.25	A	Auto recovery
Set point accuracy		1.5		%	
Line regulation		0.1	0.2	%	Low line to high line
Load regulation		0.1	0.2	%	No CD resistor
Load regulation (at VTM output)		1.0	2.0	%	Adaptive Loop
Efficiency					
Full load	93	95.6		%	See Figure 4,5 & 6
Output overvoltage set point	56		59.4	Vdc	
Output ripple voltage					
No external bypass		1.8	2.7	%	Factorized Bus, see Figure 16
With 10 µF capacitor		0.6	0.9	%	Factorized Bus, See Figure 17
Switching frequency	1.2	1.3	1.45	MHz	
Output turn-on delay					
From application of power		94	144	ms	See Figure 1
From PC pin high		100		µs	See Figure 2
Internal output capacitance		5		µF	Ceramic
Factorized Bus capacitance			47	µF	

EMI

Standard	Test Procedure	Notes
MIL-STD-461E/F		
Conducted Emissions	CE101-4	Navy ASW & Army Aircraft, Curve #2 (28 Vdc)
	CE102-1	Basic curve, for all applications
Conducted Susceptability	CS101-1	Curve #2, for all applications (28 Vdc)
	CS114-1	Conducted suceptibility, bulk cable injection, 10 KHz - 200 MHz, Curve #4
	CS115-1	Conducted suceptibility, bulk cable injection, impulse excition, all applications

INPUT WAVEFORMS & TEST CIRCUIT

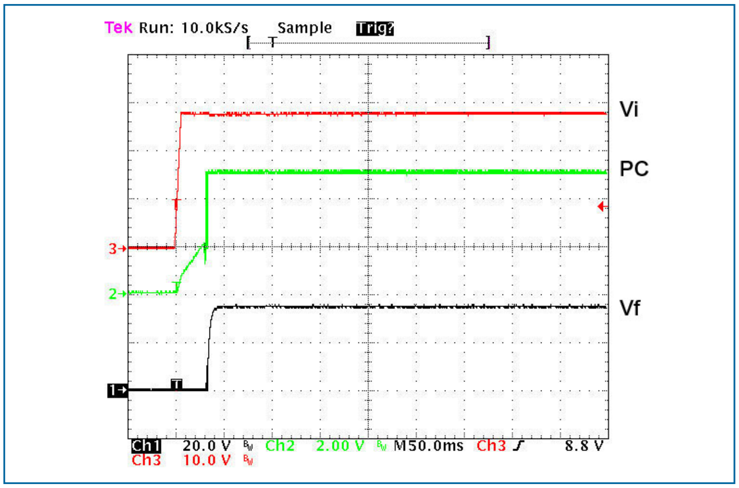


Figure 1 — *Vf and PC response from power up*

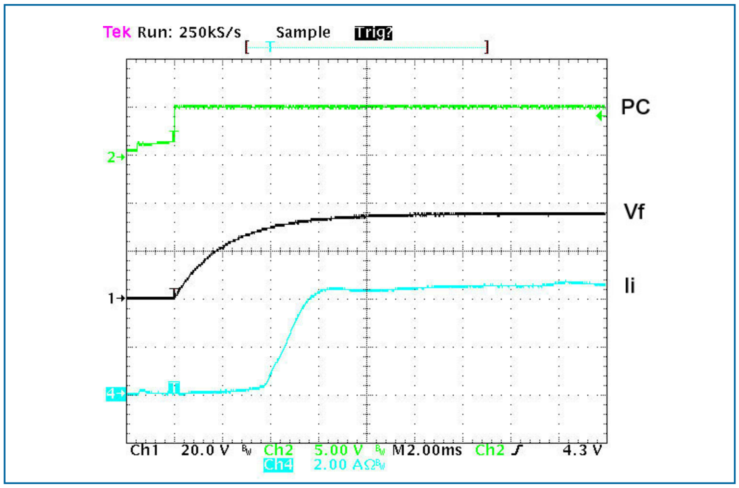


Figure 2 — *Vf turn-on waveform with inrush current – PC enabled at full load, 28 Vin, electronic load set @constant R.*

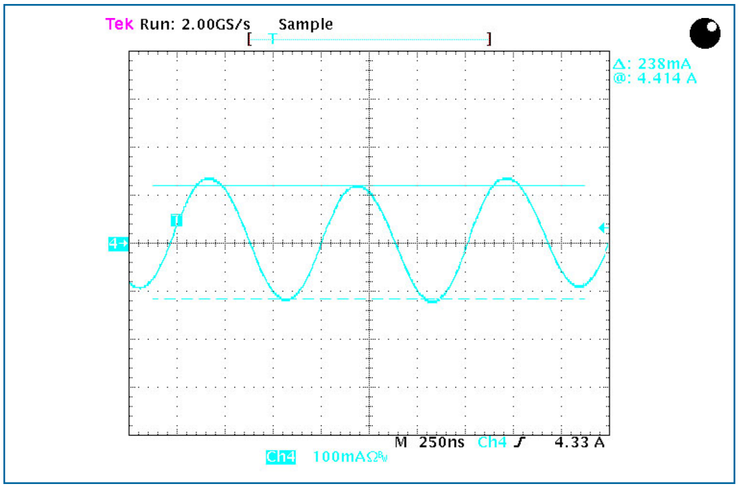


Figure 3 — *Input reflected ripple current at full load and 28 Vin*

EFFICIENCY GRAPHS

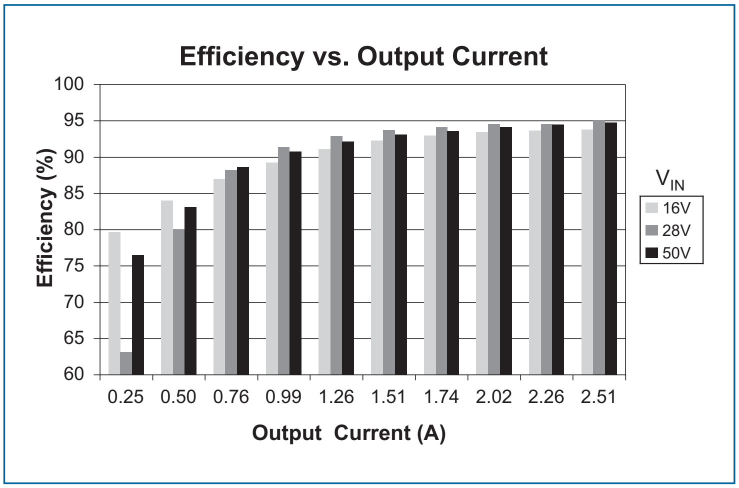


Figure 4 — Efficiency vs. output current at 48 Vf

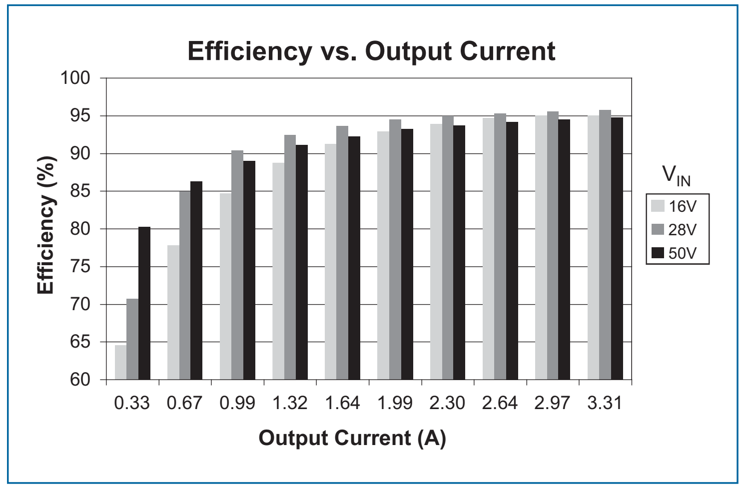


Figure 5 — Efficiency vs. output current at 36 Vf

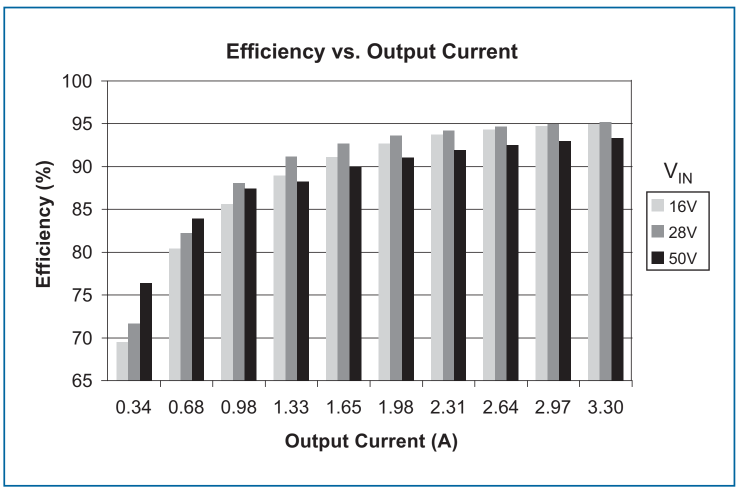


Figure 6 — Efficiency vs. output current at 26 Vf

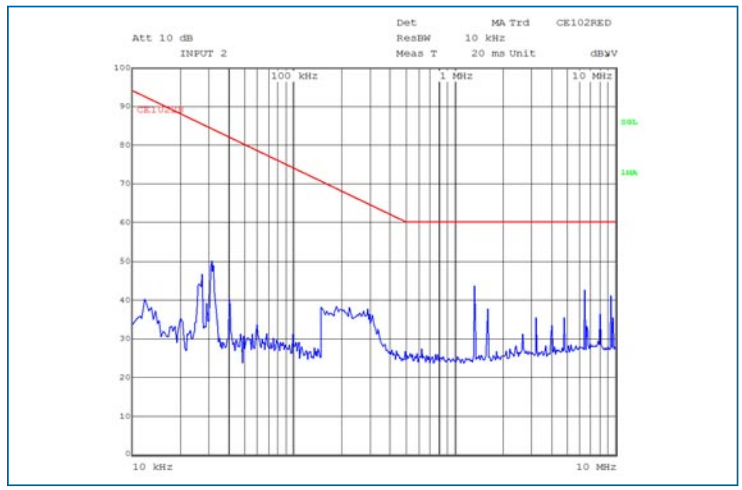


Figure 7 — Conducted Noise (CE 102); MR028B036M012FPT with VTM, 28 Vdc input, 12 Vdc output, 90% load.

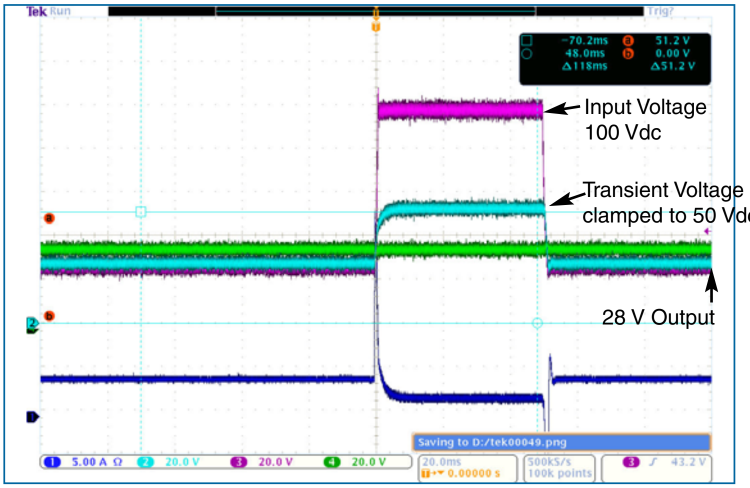


Figure 8 — *Transient immunity; MR028B036M012FPT output response to an input transient.*

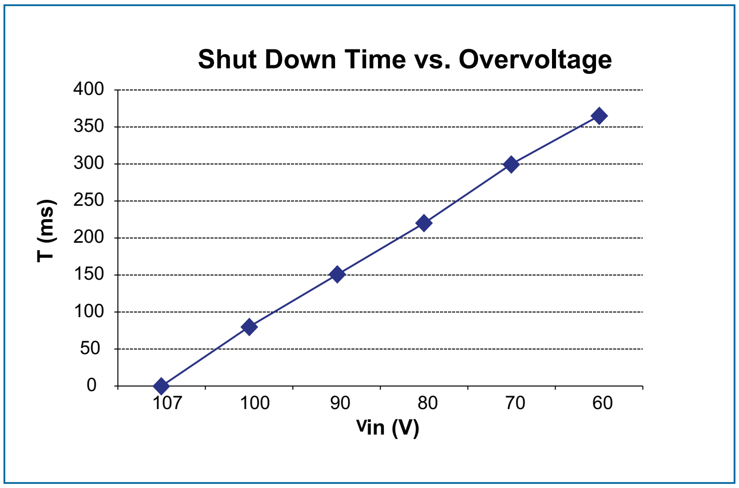


Figure 9 — *Shutdown Time vs. Overvoltage*

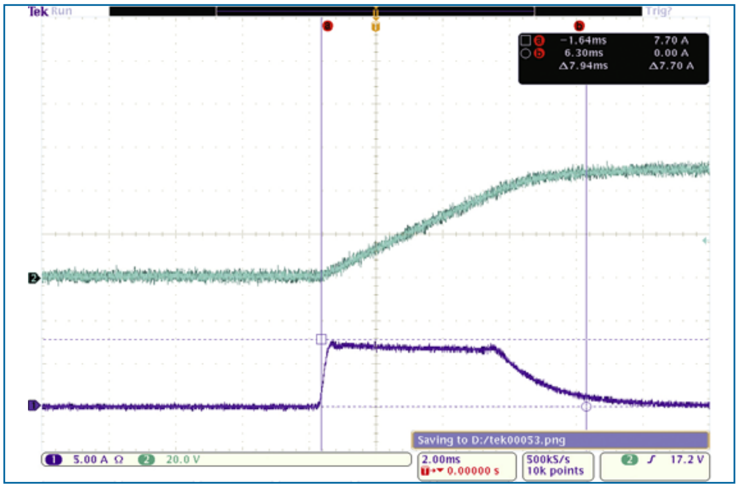


Figure 10 — *Inrush Limiting*

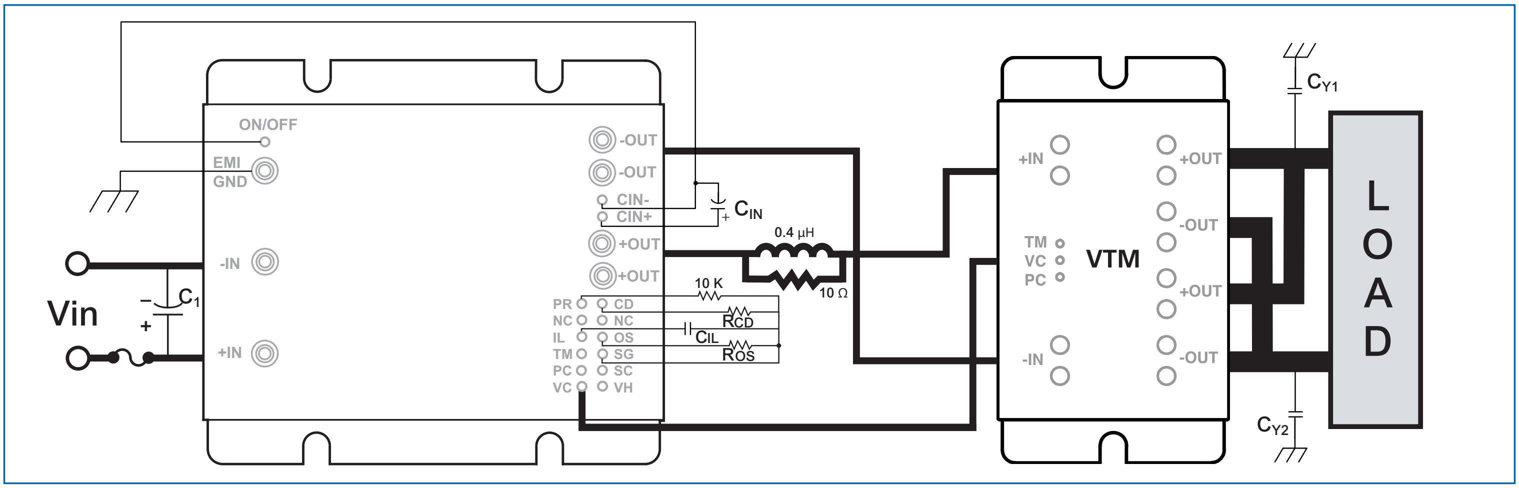


Figure 11 — *Recommended Circuit for EMI*

OUTPUT WAVEFORMS

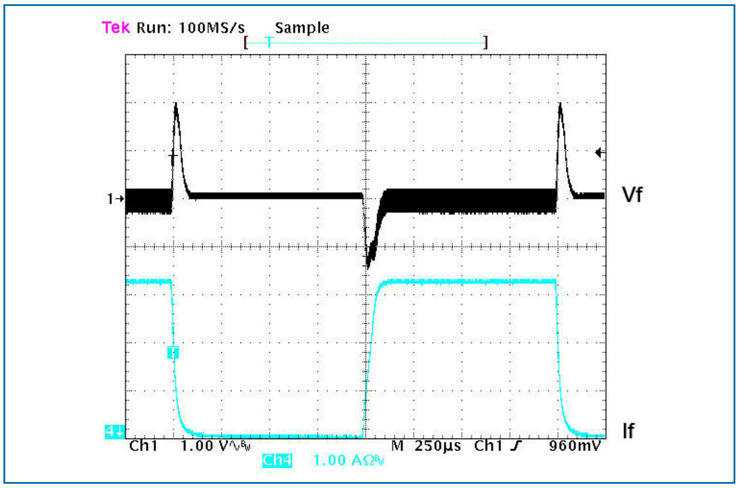


Figure 12 — *Transient response; PRM alone 28 Vin, 0-3.3-0A, no load capacitance, local loop*

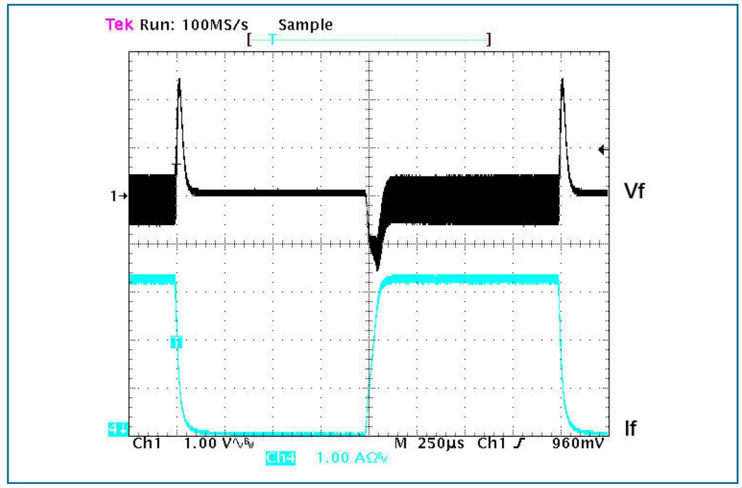


Figure 13 — *Transient response; PRM alone 16 Vin, 0-3.3-0A no load capacitance, local loop*

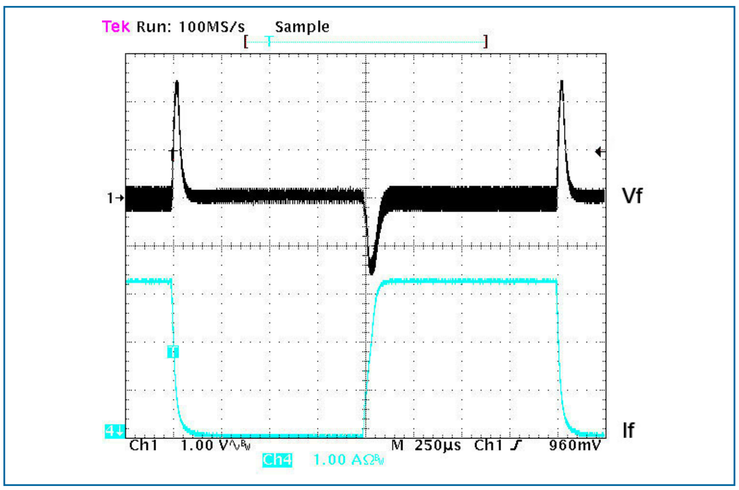


Figure 14 — *Transient response; PRM alone 50 Vin, 0-3.3-0A no load capacitance, local loop.*

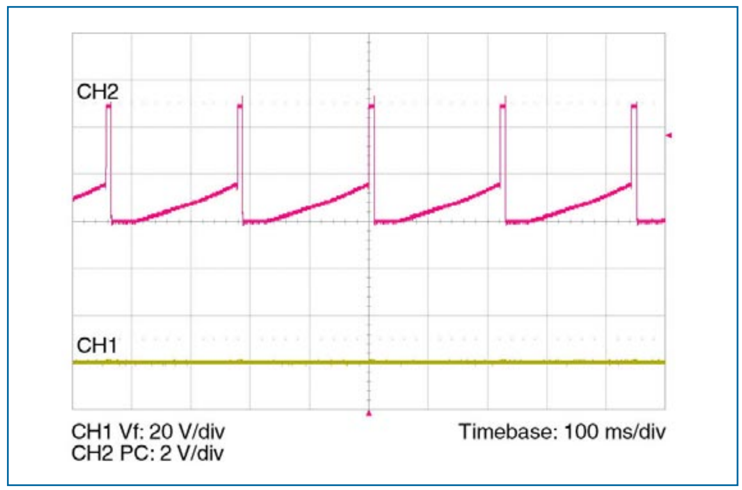


Figure 15 — *PC during fault – frequency will vary as a function of line voltage*

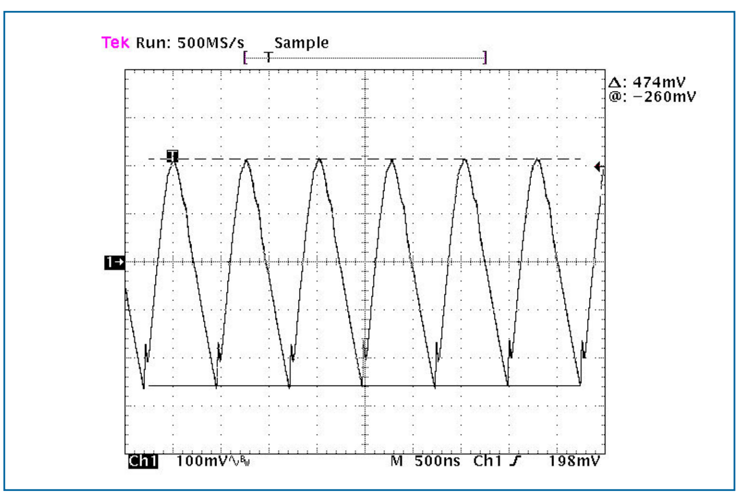


Figure 16 — *Output ripple 36 Vf, full load no bypass capacitance*

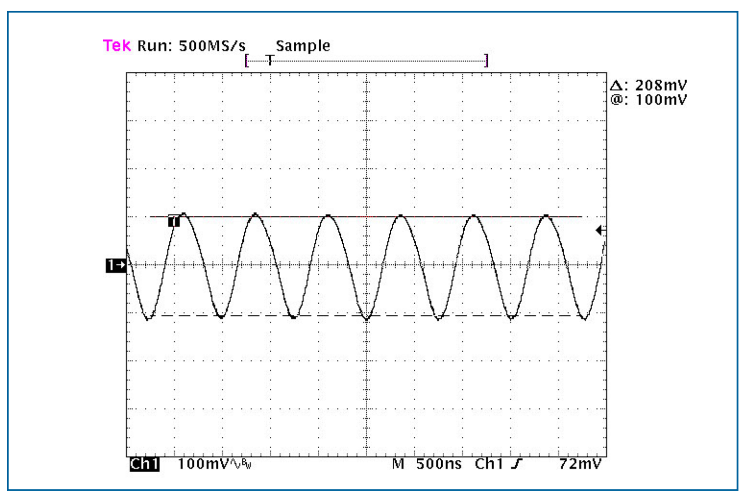


Figure 17 — *Output ripple 36 Vf, full load 10 µF bypass capacitance*

General Specifications

Parameter	Min	Typ	Max	Unit	Notes
MTBF					
MIL-HDBK-217F		2,731,720		hrs	25°C, GB
		491,573		hrs	50°C, NS
		385,172		hrs	65°C, AIC
Agency approvals		CE Mark			Low voltage directive (10 A external fuse required), EN60950-1
Mechanical parameters					See Mechanical Drawings, Figures 20 & 21
Weight		2.19 / 62,1		oz/g	
Dimensions					
Length		2.19 / 55,7		in / mm	
Width		1.91 / 48,6		in / mm	
Height		0.37 / 9,5		in / mm	
Thermal					
Over temperature shut down	130	135	140	°C	junction temperature
Thermal capacity		23.8		Ws/°C	
Baseplate to ambient		8.8		°C/W	
Baseplate to ambient; 1000 LFM		3.0		°C/W	
Baseplate to sink; flat, greased surface		0.40		°C/W	
Baseplate to sink; thermal pad		0.36		°C/W	

Auxiliary Pins

Parameter	Min	Typ	Max	Unit	Notes
C_{IN+} C_{IN-}					
EMI GND					
ON / OFF					
VC (VTM Control)					
Pulse width	8	12	18	ms	
Peak voltage		14	18	V	Referenced to –Out
PC (Primary Control)					
DC voltage	4.8	5.0	5.2	Vdc	Referenced to C_{IN}-
Module disable voltage	2.3	2.4		Vdc	Referenced to C_{IN}-
Module enable voltage		2.5	2.6	Vdc	
Disable hysteresis		100		mV	
Current limit		1.75	1.90	mA	Source only after start up; not to be used for aux. supply; 100 kΩ min. load impedance to assure start up.
Enable delay time		100		µs	
Disable delay time		1		µs	
IL (Current Limit Adjust)					
Voltage	0.95	1	1.05	V	
Accuracy		± 15		%	Based on DC current limit set point
PR					Terminate with 10 kΩ to SG
VH (Auxiliary Voltage)					Typical internal bypass C=0.1 µF
Range	8.7	9.0	9.3	Vdc	Maximum external C=0.1 µF, referenced to SG
Regulation		0.04		%/mA	
Current			5	mA p	
SC (Secondary Control)					
Voltage	1.23	1.24	1.25	Vdc	Referenced to SG
Internal capacitance		0.22		µF	
External capacitance			0.7	µF	
OS (Output Set)					
Set point accuracy		± 1.5		%	Includes 1% external resistor
Reference offset		± 4		mV	
CD (Compensation Device)					
External resistance	20			Ω	Omit resistor for regulation at output of PRM

+In / -In DC Voltage Ports

The VI BRICK maximum input voltage should not be exceeded. PRMs will turn on when the input voltage rises above its undervoltage lockout. PC will toggle indicating an out of bounds condition.

ON / OFF Pin

The module is enabled when the ON / OFF pin is connected to C_{IN}. ON / OFF pin can be connected to a 4.7 k resistor to -OUT pin to enable the module. The module is disabled when the ON / OFF pin is open circuit (floating).

+Out / -Out Factorized Voltage Output Ports

These ports provide the Factorized Bus voltage output. The –Out port is connected internally to the –In port through a current sense resistor. The PRM has a maximum power and a maximum current rating and is protected if either rating is exceeded. Do not short –Out to –In.

VC – VTM Control

The VTM Control (VC) port supplies an initial V_{CC} voltage to downstream VTMs, enabling the VTMs and synchronizing the rise of the VTM output voltage to that of the PRM. The VC port also provides feedback to the PRM to compensate for voltage drop due to the VTM output resistance. The PRM's VC port should be connected to the VTM VC port. A PRM VC port can drive a maximum of two (2) VTM VC ports.

PC – Primary Control

The PRM voltage output is enabled when the PC pin is open circuit (floating). To disable the PRM output voltage, the PC pin is pulled low. Open collector optocouplers, transistors, or relays can be used to control the PC pin. When using multiple PRMs in a high power array, the PC ports must be tied together to synchronize their turn on. During an abnormal condition the PC pin will pulse (Fig.15) as the PRM initiates a restart cycle. This will continue until the abnormal condition is rectified. The PC should not be used as an auxiliary voltage supply, nor should it be switched at a rate greater than 1 Hz.

TM – Factory Use Only

IL – Current Limit Adjust

The PRM has a preset, maximum, current limit set point. The IL port may be used to reduce the current limit set point to a lower value. The IL port must be connected to a 0.01 μF capacitor to set pin in order to prevent the noise from interfering PRM during the transient surge. See "adjusting current limits" on page 11.

PR – Factory use only

VH – Auxiliary Voltage

VH is a gated (e.g. mirrors PC), non-isolated, nominally 9 Volt, regulated DC voltage (see "Auxiliary Pins" specifications, on Page 7) that is referenced to SG. VH may be used to power external circuitry having a total current consumption of no more than 5 mA under either transient or steady state conditons including turn-on.

SC – Secondary Control

The load voltage may be controlled by connecting a resistor or voltage source to the SC port referenced to SG. The slew rate of the output voltage may be controlled by controlling the rate-of-rise of the voltage at the SC port (e.g., to limit inrush current into a capacitive load).

SG – Signal Ground

This port provides a low inductance Kelvin connection to –In and should be used as reference for the OS, CD, SC,VH and IL ports.

OS – Output Set

The application-specific value of the Factorized Bus voltage (Vf) is set by connecting a resistor between OS and SG. Resistor value selection is shown in Table 1 on Page 9, and described on Page 10. If no resistor is connected, the PRM output will be approximately one volt.

CD – Compensation Device

Adaptive Loop control is configured by connecting an external resistor between the CD port and SG. Selection of an appropriate resistor value (see Equation 2 on Page 9 and Table 1 on Page 8) configures the PRM to compensate for voltage drops in the equivalent output resistance of the VTM and the PRM-VTM distribution bus. If no resistor is connected to CD, the PRM will be in Local Loop mode and will regulate the +Out / –Out voltage to a fixed value.

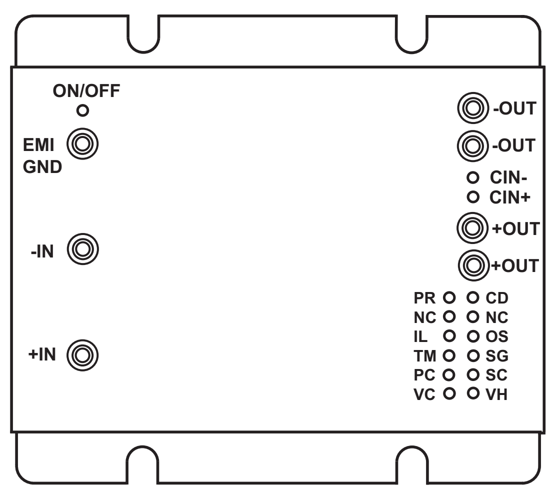


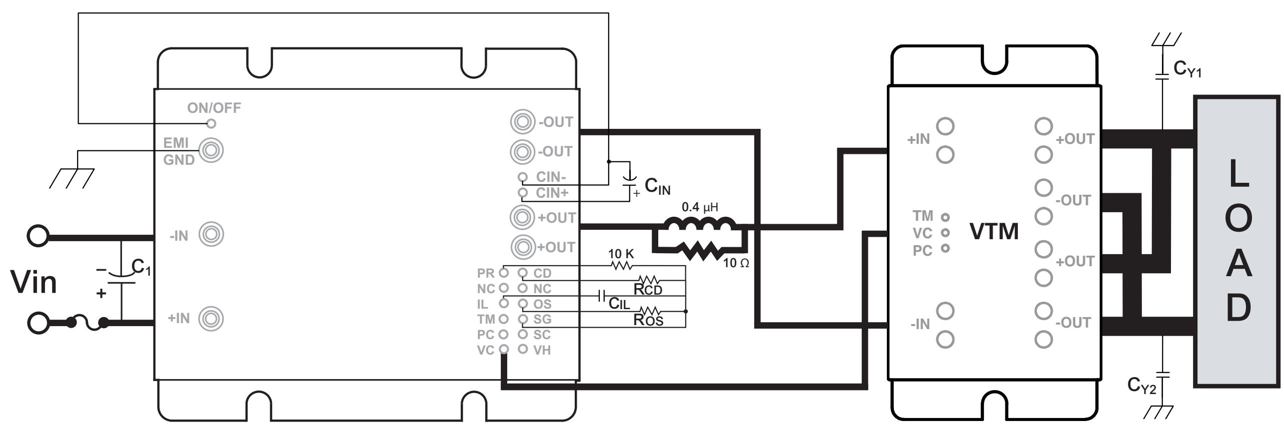
Figure 18— *MR028B036M012FPT pin configuration (viewed from pin side)*

Overview of Adaptive Loop Compensation

Adaptive Loop compensation, illustrated in Figure 11, contributes to the bandwidth and speed advantage of Factorized Power. The PRM monitors its output current and automatically adjusts its output voltage to compensate for the voltage drop in the output resistance of the VTM. R_{OS} sets the desired value of the VTM output voltage, Vout; R_{CD} is set to a value that compensates for the output resistance of the VTM (which, ideally, is located at the point of load). For selection of R_{OS} and R_{CD}, refer to Table 1 below or Page 10.

The VI BRICK's bi-directional VC port :

1. Provides a wake up signal from the PRM to the VTM that synchronizes the rise of the VTM output voltage to that of the PRM.
2. Provides feedback from the VTM to the PRM to enable the PRM to compensate for the voltage drop in VTM output resistance, R_O.



Part	Description	Value
C_1	Recommended input capacitor	10 µF / 250 V
C_{IN}	Recommended external capacitor	1000 µF / 63 V
C_{IL}	Filtering capacitor	0.01 µF
C_{Y1}, C_{Y2}	Y-type capacitor	4700 pF

Figure 19 — With Adaptive Loop control, the output of the VTM is regulated over the load current range with only a single interconnect between the PRM and VTM and without the need for isolation in the feedback path.

Desired Load Voltage (Vdc)	VI BRICK VTM P/N(1)	Max VTM Output Current (A)(2)	R_{OS} (kΩ)(3)	R_{CD} (Ω)(3)
1.0	MT036A011M100FP	100	2.70	34.8
1.2	MT036A011M100FP	100	2.24	41.2
1.5	MT036A015M080FP	80	2.39	32.4
1.8	MT036A015M080FP	80	1.98	38.3
2.0	MT036A022M055FP	55	2.70	23.2
3.3	MT036A030M040FP	40	2.16	37.4
5.0	MT036A045M027FP	27	2.14	39.2
10	MT036A090M013FP	13.3	2.14	41.2
12	MT036A120M010FP	10	2.39	21.5
15	MT036A180M007FP	6.7	2.87	34.8
24	MT036A240M005FP	5.0	2.39	38.3
28	MT036A240M005FP	5.0	2.04	41.2
36	MT036A360M003FP	3.3	2.39	34.8
48	MT036A360M003FP	3.3	1.78	45.3

Note:
(1) See Table 2 on Page 10 for nominal Vout range and K factors.
(2) See "PRM output power vs. VTM output power" on Page 11
(3) 1% precision resistors recommended

***Table 1** — Configure your Chip Set using the VI BRICK PRM.*

Output Voltage Setting with Adaptive Loop

The equations for calculating R_{OS} and R_{CD} to set a VTM output voltage are:

$$R_{OS} = \frac{69800}{\left(\frac{V_L \bullet 0.8395}{K}\right) - 1} \qquad (1)$$

$$R_{CD} = \frac{68404}{R_{OS}} + 1 \qquad (2)$$

V_L = Desired load voltage

V_{OUT} = VTM output voltage

K = VTM transformation ratio
(available from appropriate VTM data sheet)

V_f = PRM output voltage, the Factorized Bus (see Figure 19)

R_O = VTM output resistance
(available from appropriate VTM data sheet)

I_L = Load Current
(actual current delivered to the load)

Output Voltage Trimming (optional)

After setting the output voltage from the procedure above the output may be margined down (26 Vf min) by a resistor from SC-SG using this formula:

$$R_d\Omega = \frac{10000\ V_{fd}}{V_{fs} - V_{fd}}$$

Where V_{fd} is the desired factorized bus and V_{fs} is the set factorized bus.

A low voltage source can be applied to the SC port to margin the load voltage in proportion to the SC reference voltage.

An external capacitor can be added to the SC port as shown in Figure 19 to control the output voltage slew rate for soft start.

Nominal Vout Range (Vdc)	VTM K Factor
0.8 ↔ 1.6	1/32
1.1 ↔ 2.0	1/24
1.7 ↔ 3.1	1/16
2.2 ↔ 4.1	1/12
3.3 ↔ 6.2	1/8
4.3 ↔ 8.3	1/6
5.2 ↔ 10.0	1/5
6.5 ↔ 12.5	1/4
8.7 ↔ 16.6	1/3
13.0 ↔ 25.0	1/2
17.4 ↔ 33.3	2/3
26.0 ↔ 50.0	1

Table 2 *— 036 input series VTM K factor selection guide*

OVP – Overvoltage Protection

The output Overvoltage Protection set point of the MR028B036M012FPT is factory preset for 56 V. If this threshold is exceeded the output shuts down and a restart sequence is initiated, also indicated by PC pulsing. If the condition that causes OVP is still present, the unit will again shut down. This cycle will be repeated until the fault condition is removed. The OVP set point may be set at the factory to meet unique high voltage requirements.

PRM Output Power Versus VTM Output Power

As shown in Figure 20, the MR028B036M012FPT is rated to deliver 3.3 A maximum, when it is delivering an output voltage in the range from 26 V to 36 V, and 120 W, maximum, when delivering an output voltage in the range from 36 V to 50 V. When configuring a PRM for use with a specific VTM, refer to the appropriate VTM data sheet. The VTM input power can be calculated by dividing the VTM output power by the VTM efficiency (available from the VTM data sheet). The input power required by the VTM should not exceed the output power rating of the PRM.

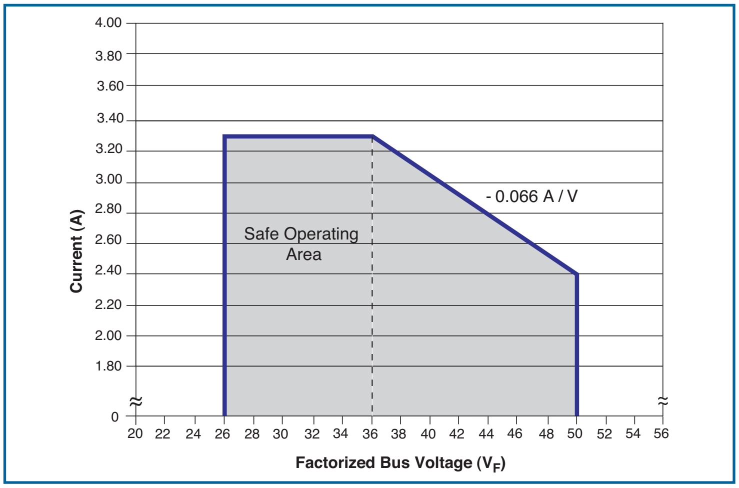


Figure 20 *— MR028B036M012FPT rating based on Factorized Bus voltage*

The Factorized Bus voltage should not exceed an absolute limit of 50 V, including steady state, ripple and transient conditions. Exceeding this limit may cause the internal OVP set point to be exceeded.

Adjusting Current Limit

The current limit can be lowered by placing an external resistor between the I_L and SG ports (see Figure 21 for resistor values). With the I_L port open-circuit, the current limit is preset to be within the range specified in the output specifications table on Page 2.

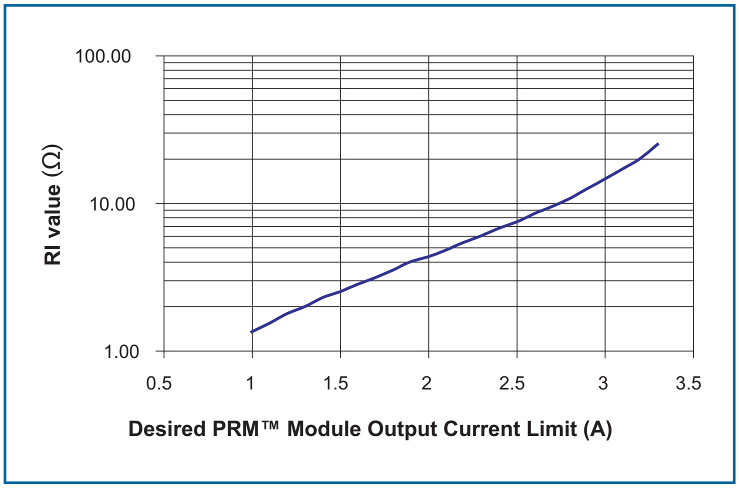


Figure 21 *— Calculated external resistor value for adjusting current limit, actual value may vary.*

Input Fuse Recommendations

A fuse should be incorporated at the input to the PRM, in series with the +In port. A fast acting fuse, NANO2 FUSE 451/453 Series 10 A 125 V, or equivalent, may be required to meet certain safety agency Conditions of Acceptability. Always ascertain and observe the safety, regulatory, or other agency specifications that apply to your specific application. For agency approvals and fusing conditions, click on the link below:

http://www.vicorpower.com/technical_library/technical_documentation/quality_and_certification/safety_approvals/

Application Notes

For PRM and VI BRICK application notes on soldering, board layout, and system design please click on the link below:

http://www.vicorpower.com/technical_library/application_information/

Applications Assistance

Please contact Vicor Applications Engineering for assistance, 1-800-927-9474, or email at apps@vicorpower.com.

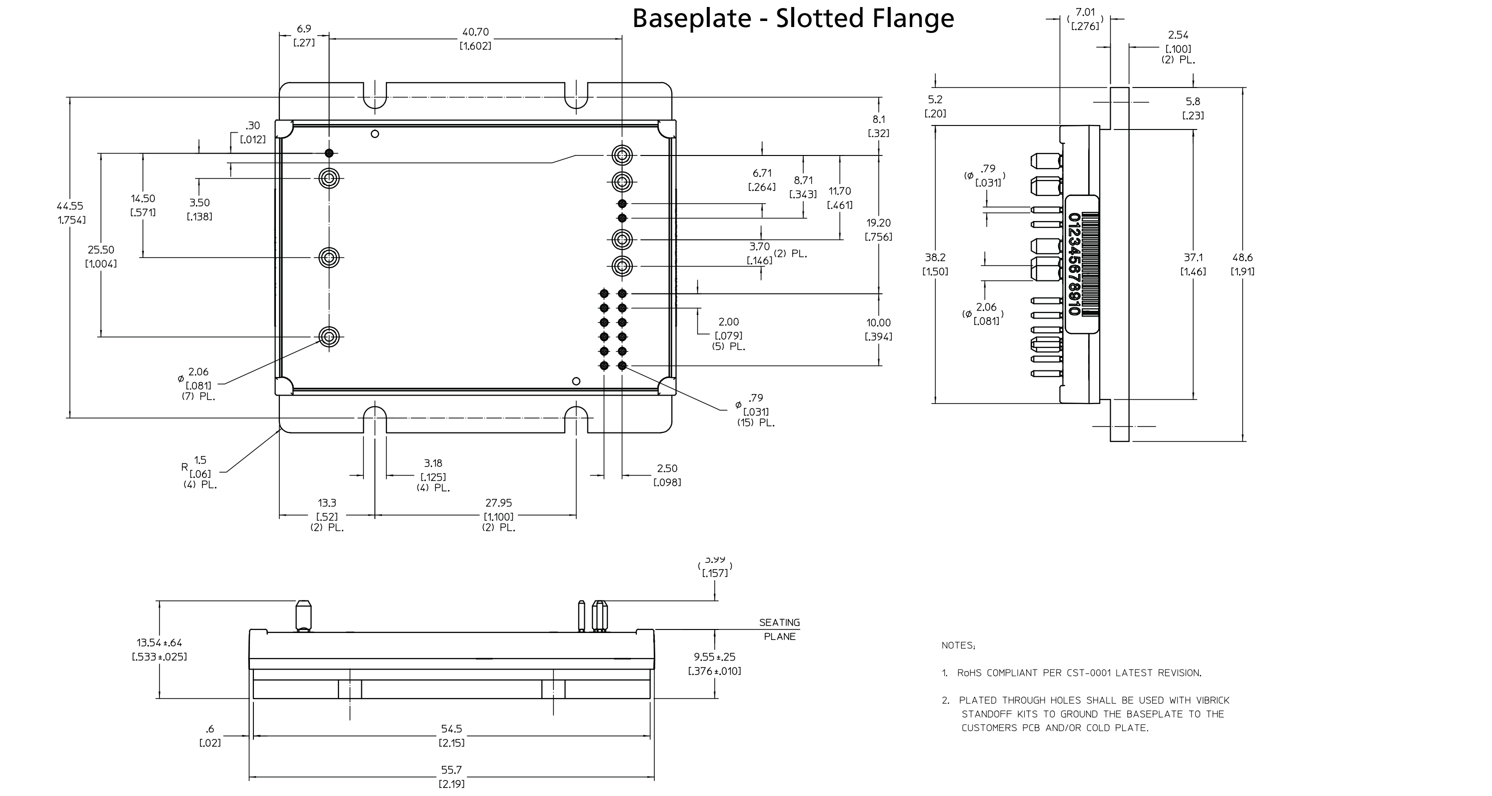


Figure 22 *— Module outline*

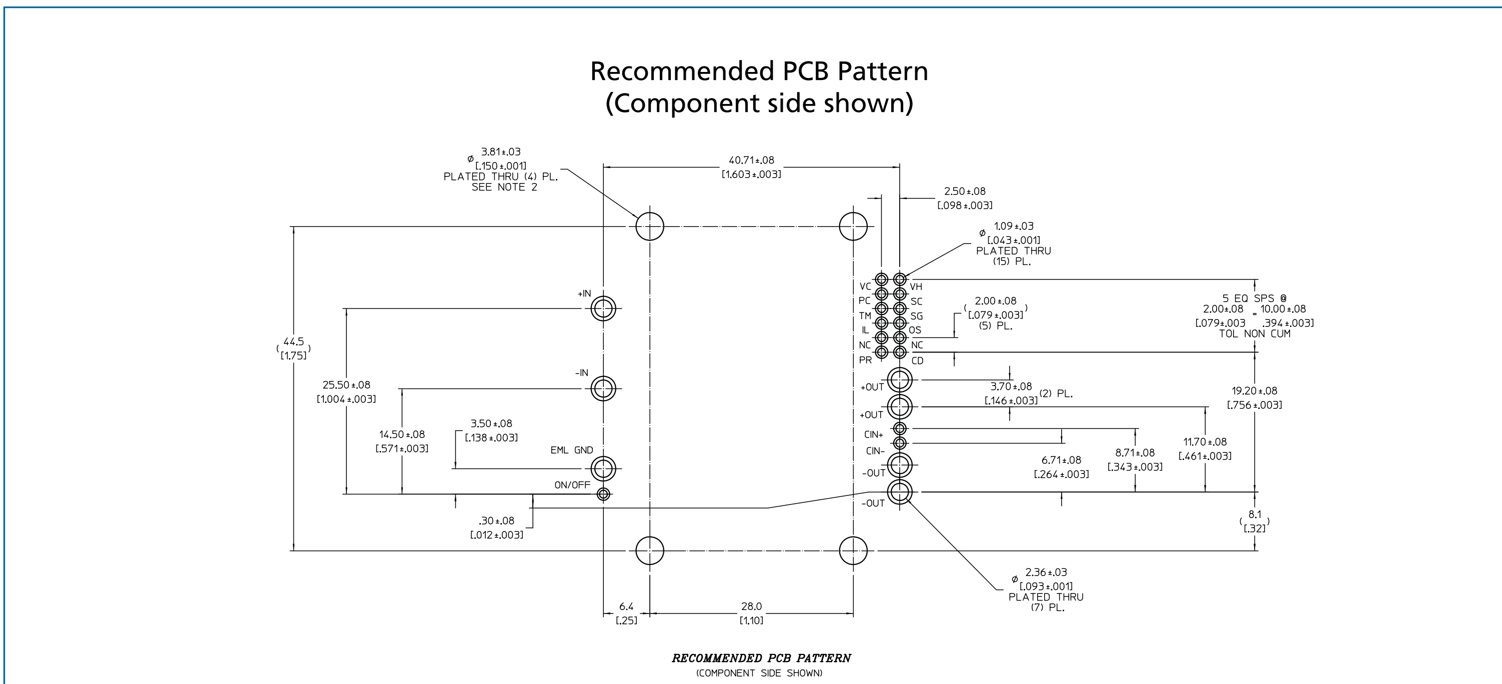


Figure 23 *— PCB mounting specifications*

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