

High Voltage BCM™ Parallel Array System User’s Guide

| | |
|--|-------------|
| Contents | Page |
| 1.0 Introduction | 1 |
| 1.1 Note on System Components | 1 |
| 1.2 Features | 1 |
| 2.0 Evaluation System Description | 2 |
| 2.1 High Voltage BCM Parallel Array | |
| 2.1.1 Power Rating of BCM Parallel Array | |
| 2.1.2 High Voltage BCM Parallel Array Components | 3 |
| 2.1.3 High Voltage BCM Parallel Array Schematic | 4 |
| 2.1.4 High Voltage BCM Parallel Array Layout | 5 |
| 2.2 High Voltage BCM Parallel Evaluation Board | 6 |
| 2.2.1 High Voltage Parallel Evaluation Baseboard Components | |
| 2.2.2 High Voltage Parallel Evaluation Baseboard Schematic | 7 |
| 2.2.3 High Voltage Parallel Evaluation Baseboard Layout | |
| 2.3 High Voltage BCM Parallel Array System Bill of Material | 8 |
| 2.3.1 High Voltage BCM Parallel Array Bill of Material | |
| 2.3.2 High Voltage BCM Evaluation Baseboard Bill of Material | |
| 3.0 Using the High Voltage BCM Parallel Array Evaluation System Hardware | 8 |
| 3.1 Warning | |
| 3.2 Mounting Heat Sinks | 10 |
| 3.3 Array / Baseboard Interface | |
| 3.4 Load Connection | |
| 3.3 Line Connection | 11 |
| 3.4 Power Up Procedure | |
| 3.5 Evaluation System Basic DO's & DON'ts | |
| 4.0 Basic Laboratory Test Procedures | 11 |
| 4.1 Measuring Efficiency | |
| 4.2 Output Voltage Ripple | 12 |
| 4.3 Enable / Disable Timing | |
| 4.4 Thermal Testing | 14 |
| 5.0 Conclusion | 15 |

Warning

Read all precautions throughout the guide BEFORE using the High Voltage BCM Parallel Array Evaluation System. Do not operate the High Voltage BCM Parallel Array Evaluation System unless you have the appropriate safety precautions in place on your bench to guarantee safety. The user's guide is not comprehensive and is not a substitute for common sense and good practice.

1.0 Introduction

The High Voltage BCM Array System is a two piece evaluation system for powering, testing, and using high voltage input V•I Chip BCMs in a high power array. The system includes a vertical mounted card containing 4 BCMs connected with inputs and outputs in parallel as well as a horizontal mounted baseboard with a mating connector for the array board. The Evaluation System baseboard enables the testing of any compatible array boards and simplifies the connection of the input source and output load to the array.

1.1 Note on System Components

The High Voltage BCM Parallel Array Evaluation System contains two components:

High Voltage BCM Parallel Array refers to the vertical mounted card containing 4 BCMs (two on either side), as shown in Figure 1.

High Voltage BCM Parallel Evaluation Baseboard refers to the horizontal mounted card containing the mating connector for the array board and the input and output lug connections as shown in Figure 6.

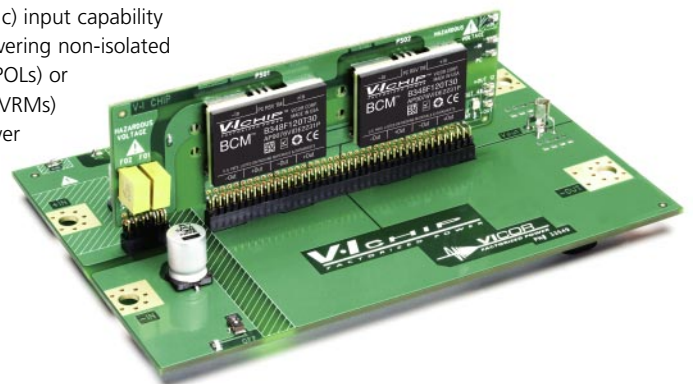
1.2 Features

The High Voltage BCM Parallel Array System contains the following:

- High Voltage BCM Parallel Array containing up to four BCMs for 1.2 kW total power
- High current output interconnect for >100 A of output current carrying capability
- Kelvin connections for measuring the efficiency of the V•I Chip components independent of load connect losses
- An oscilloscope probe jack for measuring output voltage, including output voltage ripple
- Optional pads for ceramic capacitors for evaluating output filtering
- Fused BCM inputs
- Provision for mounting optional V•I Chip push-pin heat sinks
- System enable and disable
- Output Power present indicators

The BCM Parallel Array provides the following features:

- High efficiency (>95%) DC-DC Voltage transformation
- Full line isolation 4,242 Vdc
- PFC compatible (360-400 Vdc) input capability
- Isolated 12 V output for powering non-isolated Point-of-Load Regulators (niPOLs) or Voltage Regulator Modules (VRMs)
- Surface-Mount V•I Chip power component package



2.0 Evaluation System Description

2.1 The High Voltage BCM Parallel Array

The High Voltage BCM Parallel Array contains 4 High Voltage B384F120T30 BCMs.

Please refer to the appropriate V•I Chip data sheets for product-specific information regarding the operation and maximum ratings of the individual BCMs in the array. The data sheets can be found online at:

vicorpower.com/documents/datasheets/384V_12V_300W_BCM.pdf

2.1.1 Power rating of BCM Parallel Array

The power rating of an array of BCMs is equal to the power rating of the individual BCM times the number of BCMs in an array. The High Voltage BCM Parallel Array is therefore capable of providing up to 1.2 kW of output power.

2.1.2 High Voltage BCM Parallel Array Components

Figure 1
High Voltage BCM
Parallel Array
front

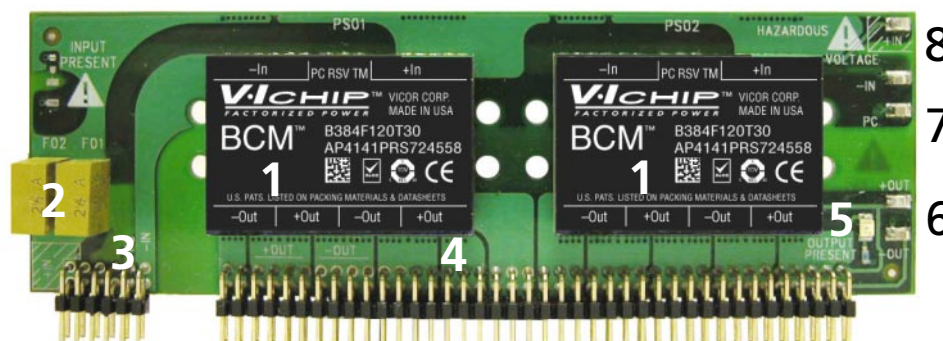


Figure 2
High Voltage BCM
Parallel Array
back

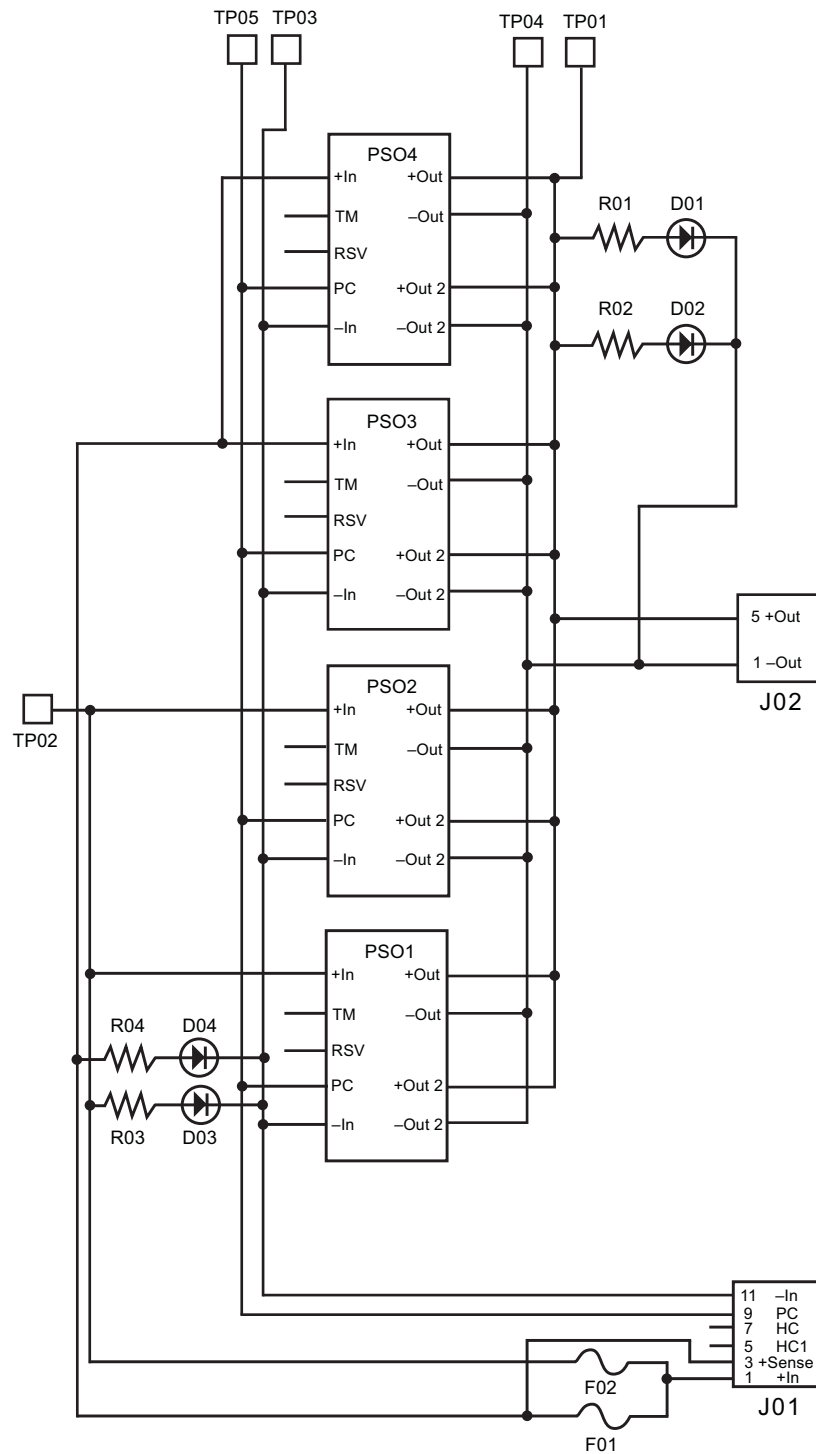


Please refer to *Figure 1* and *2* for the High Voltage BCM Parallel Array components.

1. **BCMs (PS01, PS02, PS03, PS04).** These are the BCM V•Chip components that provide the DC-DC transformation and isolation of the input power.
2. **Fuses (F01, F02).** These are High Voltage DC fuses which provide fault protection to the board. F01 fuses PS01 and PS02. F02 fuses PS03 and PS04.
3. **Input Connector (J01).** Connects to +IN and -IN on the BCM array. Provides input power. Also brings PC connection from BCM array to the baseboard.
4. **Output Connector (J02).** Connects to +Out and -Out on the BCM. Provides output current to the baseboard. Contains two kelvin pins for baseboard test points.
5. **Output Present LED (D01, D02).** Lights green when output voltage is present. Provides visual indication of BCM array operation.
6. **Output Kelvin Test Points (TP01, TP04).** Provides a voltage measurement directly on the output of BCM array to enable an accurate efficiency measurement of the V•Chips.
7. **PC (TP05).** Test point for PC signal. This signal serves as a fault flag for the BCM as well as an enable / disable signal.
8. **Input Kelvin Test Points (TP02, TP03).** Provides a voltage measurement directly on the input of the BCM array to enable an accurate efficiency measurement of the V•Chips.

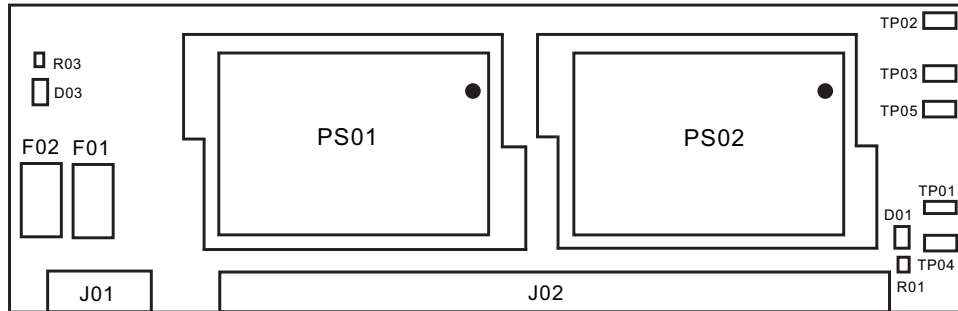
2.1.3 High Voltage BCM Parallel Array Schematic

Figure 3
High Voltage BCM
Parallel Array Schematic



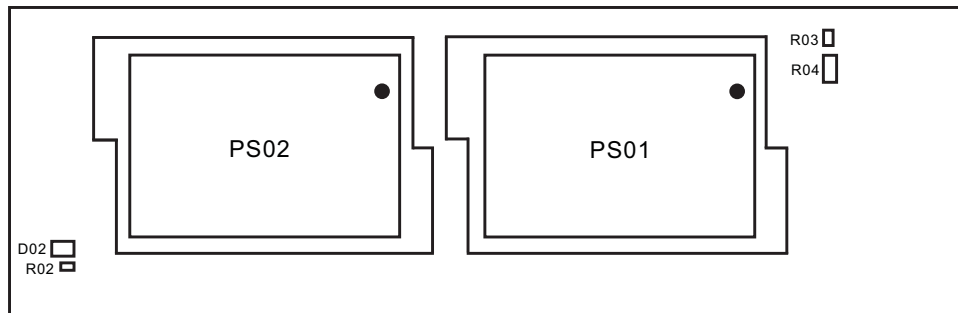
2.1.4 High Voltage BCM Parallel Array Layout

Figure 4
High Voltage BCM
Parallel Array Layout
(top)



Top View

Figure 5
High Voltage BCM
Parallel Array Layout
(bottom)



Bottom View

2.2 High Voltage BCM Parallel Evaluation Baseboard

The High Voltage BCM Evaluation Baseboard enables laboratory evaluation of the High Voltage BCM Parallel Array. It provides a stable horizontal base for the vertical array card as well as source and load interconnect lugs, a scope probe jack, and Kelvin test points for input and output voltage measurement. It also contains an enable / disable switch that toggles the array PC signal.

2.2.1 High Voltage Parallel Evaluation Baseboard Components

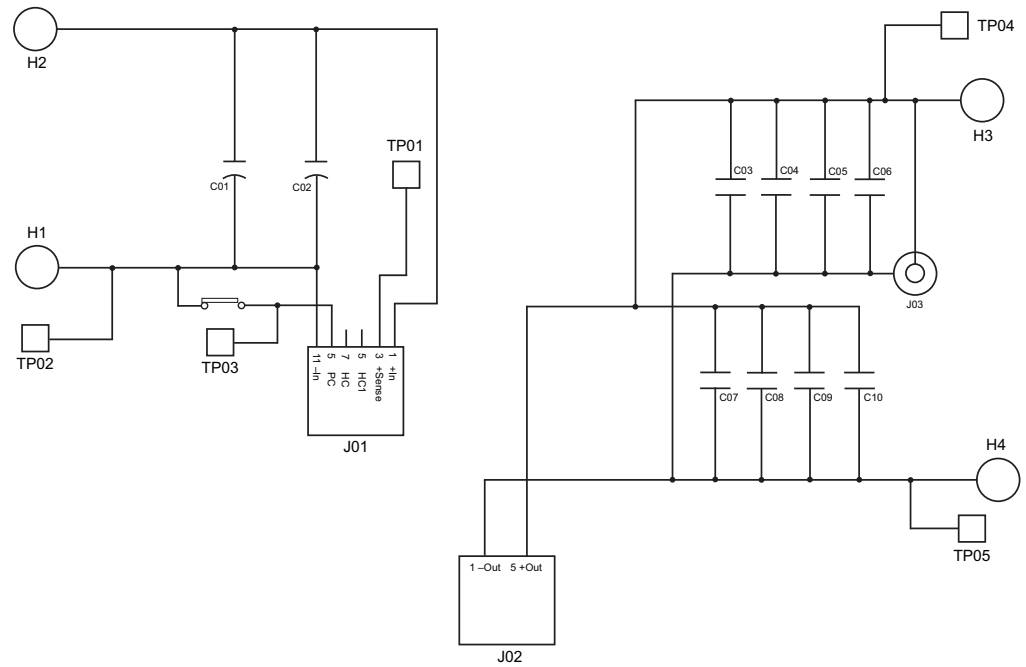
Figure 6
High Voltage BCM
Parallel Array component
placement



1. **Array Output Socket (J02).** Interfaces with the output connect on the High Voltage BCM Parallel Array.
2. **Array Input Connector (J01).** Interfaces with the input connector on the High Voltage BCM Parallel Array.
3. **Input Capacitors (C01, C02).** Provides low AC impedance at the input of the array. This enables the performance of the array to be essentially independent of the upstream source impedance, allowing longer connection wires to be used between the source and baseboard for benchtop evaluation purposes.
4. **Input Source Lugs (H1, H2).** Connect the High Voltage source (DC supply or PFC front-end output) here, using 10 – 32 size screws and lugs.
5. **Array enable / disable switch (SW01).** This switch toggles the PC signal for the array. With the switch in the “UP” position, the PC is floating and the array is enabled. With the switch in the “DOWN” position, the PC is connected to –IN and the array is disabled.
6. **PC Test Point.** Connection to the PC signal of the array. The array can be toggled ON and OFF via the PC port with an external circuit.
7. **Output Load Lugs (H3, H4).** Connect the load here (resistor bank, motherboard, or electronic load) using 10 – 32 size screws and lugs.
8. **Output Voltage Oscilloscope Probe Jack (J03).** Accepts most oscilloscope probes and enables precision measurement of the output voltage ripple.
9. **Input Kelvin Test Points.** Kelvin connections to the input of the BCM array enable accurate efficiency measurements of the V•I Chips independent of interconnect losses.
10. **Output Kelvin Test Points.** Kelvin connections to the output of the BCM array to enable accurate efficiency measurements of the V•I Chips independent of interconnect losses.
11. **Output Capacitors (C03 - C10).** Accommodations for ceramic output capacitors for output filtering. Use 1206 sized capacitors rated for at least 15 V.

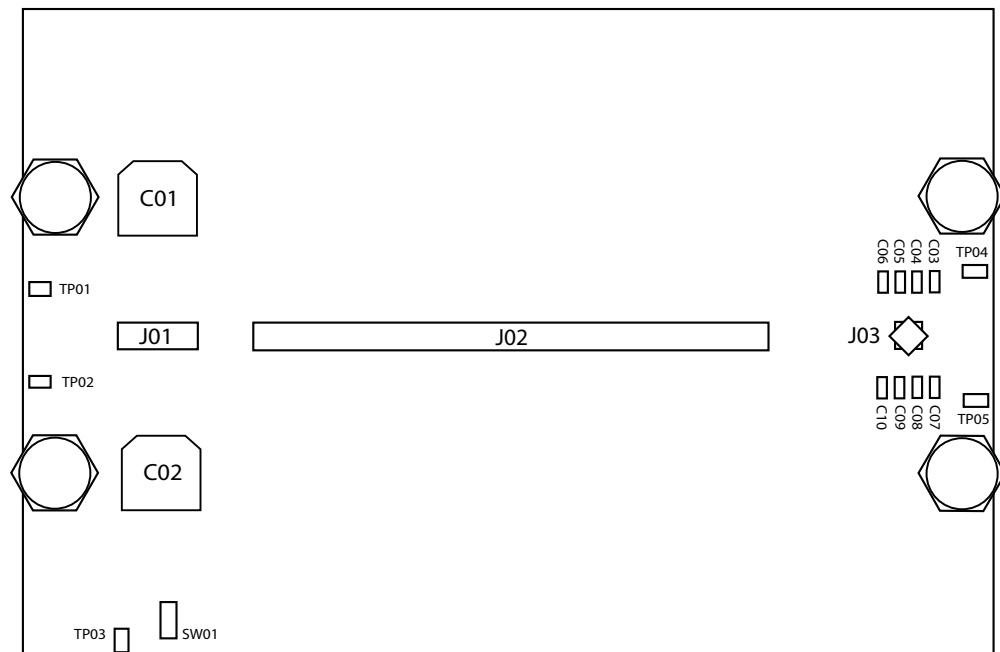
2.2.2 High Voltage BCM Parallel Array Baseboard Schematic

Figure 7
High Voltage BCM
Parallel Array
Baseboard Schematic



2.2.3 High Voltage BCM Parallel Array Baseboard Layout

Figure 8
High Voltage
BCM Parallel Array
Baseboard Layout



2.3 High Voltage BCM Parallel Array System Bill of Material

2.3.1 High Voltage BCM Parallel Array Bill of Material

| Item No. | Description | Ref. Des. | Vicor PN | Vendor | Vendor PN |
|----------|--------------------------------------|-----------|-------------|---------|--------------|
| 1 | BCM HV Array Evaluation daughtercard | PCB | 33221 | | |
| 2 | B384F120T30 V•I Chip BCM | PS1 | B384F120T30 | | |
| 3 | B384F120T30 V•I Chip BCM | PS2 | B384F120T30 | | |
| 4 | B384F120T30 V•I Chip BCM | PS3 | B384F120T30 | | |
| 5 | B384F120T30 V•I Chip BCM | PS4 | B384F120T30 | | |
| 6 | 2.5 A / 450 Vdc fuse | F01 | 08395 | | |
| 7 | 2.5 A / 450 Vdc fuse | F02 | 08395 | | |
| 8 | 0603 10 K Ohm resistor | R01 | | | |
| 9 | 0603 10 K Ohm resistor | R02 | | | |
| 10 | 1206 clear green SMT LED | D01 | | Digikey | 67-1698-1-ND |
| 11 | 1206 clear green SMT LED | D02 | | Digikey | 67-1698-1-ND |
| 12 | 12 pin right angle connector | J01 | | Digikey | S5803-06-ND |
| 13 | 80 pin right angle header | J02 | | Digikey | S5803-04-ND |
| 14 | Test point surface mount | TP01 | 27995 | | |
| 15 | Test point surface mount | TP02 | 27995 | | |
| 16 | Test point surface mount | TP03 | 27995 | | |
| 17 | Test point surface mount | TP04 | 27995 | | |
| 18 | Test point surface mount | TP05 | 27995 | | |

2.3.2 High Voltage BCM Parallel Evaluation Baseboard Bill of Material

| Item No. | Description | Ref. Des. | Vicor PN | Vendor | Vendor PN |
|----------|-----------------------------------|-----------|-----------|---------|--------------|
| 1 | BCM HV Array Evaluation Baseboard | PCB | 33549 | | |
| 2 | 12 pin right angle receptical | J01 | | Digikey | S5750--06-ND |
| 3 | 80 pin right angle receptical | J02 | | Digikey | S5750--40-ND |
| 4 | Cap Al-EL 2.2 μ F 450 V | C01 | 28506-225 | | |
| 5 | Cap Al-EL 2.2 μ F 450 V | C02 | 28506-225 | | |
| 6 | Test point surface mount | TP01 | 27995 | | |
| 7 | Test point surface mount | TP02 | 27995 | | |
| 8 | Test point surface mount | TP03 | 27995 | | |
| 9 | Test point surface mount | TP04 | 27995 | | |
| 10 | Test point surface mount | TP05 | 27995 | | |
| 11 | Scope Jack Tektronix | J03 | 16949 | | |
| 12 | SPST SMD switch | SW01 | | | |

3.0 Using the High Voltage BCM Parallel Array Evaluation System

3.1 Warning

Read the precautions below entirely **BEFORE** using the High Voltage BCM Parallel Array Evaluation System. Do not operate the High Voltage BCM Parallel Array Evaluation System unless you have the appropriate safety precautions in place on your bench to guarantee safety. **Hazardous Voltages are present on the High Voltage BCM Parallel Array Evaluation System under power. PERSONAL CONTACT WITH LINE VOLTAGE MAY RESULT IN SEVERE INJURY, DISABILITY, OR DEATH. IMPROPER OR UNSAFE HANDLING OF THIS BOARD MAY RESULT IN SERIOUS INJURY OR DEATH.** The list below is not comprehensive and is not a substitute for common sense and good practice.

1. ALWAYS remove power before touching, servicing, or attaching probes to the system. Verify that the power is removed before touching. Physically disconnect input power or use a lockout / tagout (LOTO) system to prevent the accidental application of power while servicing the High Voltage BCM Parallel Array Evaluation System. Ensure input caps are fully discharged.
2. The system is designed to demonstrate the use of BCMs in offline systems. For general laboratory evaluation, it is highly recommended, for safety purposes, to use an isolated high voltage source for the system. This source can be a benchtop regulated high voltage DC source, or an offline PFC front-end powered through an ISO-VAC or line isolation transformer.

3. NEVER leave the system unattended when under power.
4. DO NOT allow other people to work in the vicinity of the system under power.
5. Provide strain relief for wires and place the High Voltage BCM Parallel Array Evaluation System on the bench in such a way as to prevent accidental dislodgement from the benchtop. Connecting wires or attached probes should not hang off the bench.
6. NEVER probe the input of the High Voltage BCM Evaluation System with a non-isolated oscilloscope probe unless absolutely sure of whether or not the input is line isolated.
7. USE appropriate shielding of exposed high voltage areas of the system to prevent accidental casual contact. Please refer to Figure 9, 10, 11 for a map of the exposed high voltage areas on both sides of the board.

Figure 9
Exposed hazardous voltage
High Voltage BCM Array
top

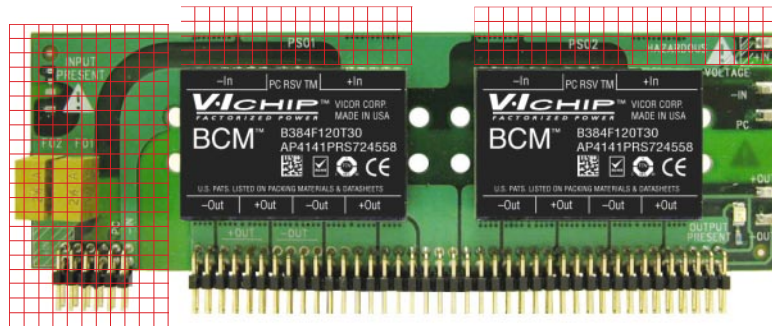


Figure 10
Exposed hazardous voltage
High Voltage BCM Array
bottom

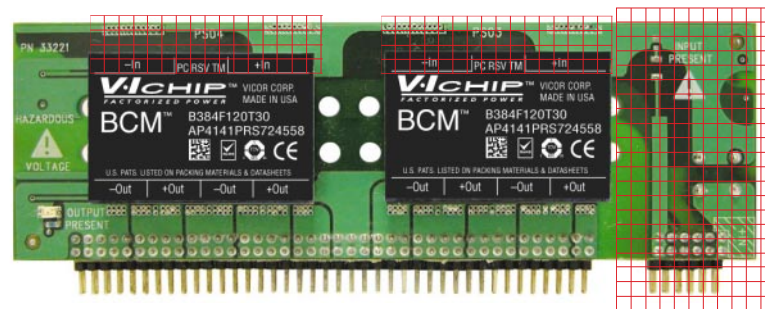
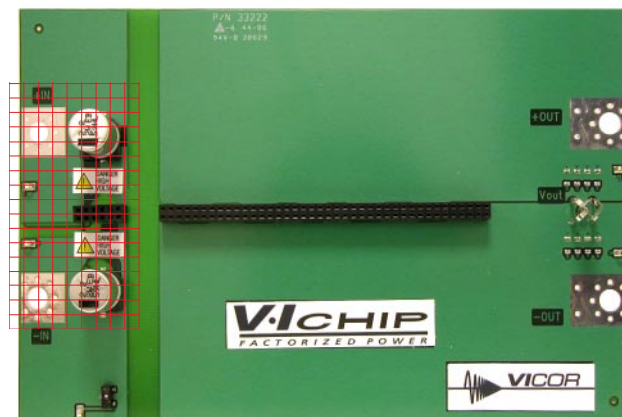


Figure 11
Exposed hazardous voltage
High Voltage Evaluation
Baseboard



8. NEVER jumper across the fuses on the High Voltage BCM Parallel Array Evaluation System. Replace fuses only with fuses of equivalent type and rating.
9. The High Voltage BCM Parallel Array Evaluation System is designed for use in a laboratory environment. Use of the system in other environments is not recommended. The High Voltage Evaluation Baseboard should always be mounted to a flat surface, and wired in such a way that it rests firmly on the bench.

10. **DO NOT** attempt to wire or use the High Voltage BCM Parallel Array without the baseboard or an equivalent connector.
11. **NEVER** attempt to disconnect the array from the baseboard while power is applied. This system is not designed to demonstrate hot plug capability. Additional components would be required to implement a hot plug capable system.

3.2 Mounting Heat Sinks

Push-pin V.I. Chip heat sinks are included with the High Voltage BCM Parallel Array to allow extended benchtop testing at full power and lower airflow. Please follow the procedure below when mounting heat sinks to the BCMs.

1. Place the High Voltage BCM Parallel Array on a flat benchtop with the top side facing up. The board should be resting on the bottom BCMs. Verify that the board is flat, and there are no obstructions under the board or near the hole location.
2. Make sure the top of the BCMs are clean and free of dust or debris.
3. Place a heat sink on top of the first BCM and align the push pins with the appropriate holes. Push lightly on the heat sink to engage the thermal interface with the case of the V.I. Chip.
4. With the top of a pen press firmly on each push-pin until it engages in the hole. The push-pin should click and lock firmly into the hole. Do not force the push-pin, and do not apply more than 5 lbs. pressure to engage the pin.
5. Repeat step #4 with the second heat sink on the top side.
6. Turn the High Voltage BCM Parallel Array over and repeat steps #2-#5 for the remaining two heat sinks.

If, for any reason, the heat sinks need to be removed, cut the push-pins with a pair of snips or wire cutters. Do not attempt to preserve the push-pins for re-use. The heat sink push-pins can be replaced (please see the Vicor catalog for part numbers and ordering information) and the heat sink itself re-used if desired.

3.3 Array / Baseboard Interface

The High Voltage BCM Parallel Array connects to the High Voltage Evaluation Baseboard using a pair of standard 2 mm pitch pin connectors. The following guidelines should be followed when connecting and disconnecting the array from the baseboard.

Improper handling of the High Voltage BCM Parallel Array Evaluation System can result in injury or death.

1. The system should **always be powered off before attempting to connect or disconnect the array from the baseboard**. Input voltage should be removed (not disabled using the on / off switch). Always check to make sure that the system is off before disconnecting the two components.
2. To connect the array, align the pins of the array with the sockets on the baseboard. With one hand on either end of the board apply direct downward pressure on the array and push the pins evenly into the sockets.
Do not force the array pins into the socket. If array does not fit into the socket, check to make sure the pins are not bent. If they are, straighten them with a pair of pliers. More pressure will need to be applied to the output end of the array due to the fact that there are more pins on that side of the board. Do not insert the array into the socket by applying pressure on the BCMs; apply force directly to the board.
3. To remove the array, with one hand hold the baseboard firmly to the benchtop surface. With the other hand, grip the array close to the connector and ease it up slightly on one end. Repeat this on the other end. Keep edging the array slowly out of the connector end by end until the connection loosens and the array can be easily lifted out.

3.4 Load Connection

Note: Please refer to the BCM data sheet specifications for the applicable ratings (Input, Output Power for single BCM, voltage, etc.)

Connect a resistor, motherboard, or electronic load, capable of at least the rated power of the BCM array to + Out and -Out of the Array Evaluation Baseboard (locations shown in Figure 7).

The array will operate correctly at no load.

The output voltage may be monitored using an oscilloscope probe placed in J03 (Figure 8).

3.3 Line Connection

Improper handling of the High Voltage BCM Parallel Array Evaluation System can result in injury or death.

Connect a DC power source capable of providing at least 115% of the rated power of the BCM array to +IN and –IN of the baseboard, shown in Figure 6.

Note: Verify that all connections are made properly before applying power.

Once power is applied to the board, lethal voltages are present. Necessary precautions should be taken to avoid injury.

The use of an AC isolation transformer when using a non-isolated PFC front end is highly recommended.

3.4 Power Up Procedure

Improper handling of the High Voltage BCM Parallel Array Evaluation System can result in injury or death.

Apply DC voltage to the High Voltage BCM Parallel Array Evaluation System and verify that there is an output voltage as expected. DC voltage may be applied directly by switch action, or powered up slowly using a high voltage adjustable DC source.

3.5 Evaluation System Basic DO's and DON'ts

Improper handling of the High Voltage BCM Parallel Array Evaluation System can result in injury or death.

DO observe necessary safety precautions when using the evaluation system at all times.

DO keep a fan blowing on the High Voltage BCM Parallel Array Evaluation System when running for extended periods of time at high load, and be mindful that the heat sinks may be hot.

DO keep wires, probes, jumpers, etc. well contained and fixed when using the High Voltage BCM Parallel Array Evaluation System.

DO NOT attempt to tamper with, replace, or change components on the High Voltage BCM Parallel Array Evaluation System.

DO NOT probe, connect, or disconnect wires on the High Voltage BCM Parallel Array Evaluation System while line voltage is applied.

DO NOT exceed any of the input and output ratings of the BCM Parallel Array as specified in the single BCM data sheet. If unsure about whether or not a procedure is acceptable, please contact Vicor Applications Engineering for assistance.

4.0 Basic Laboratory Test Procedures

This section will cover some basic test procedures for acquiring data using the High Voltage BCM Parallel Array Evaluation System. Actual laboratory test data will be shared for a system using a 1.2 kW array of B384F110T30 modules.

4.1 Measuring Efficiency

The High Voltage BCM Parallel Array Evaluation System is equipped with input and output Kelvin connections to facilitate efficiency measurements. The following procedure should be followed to measure efficiency.

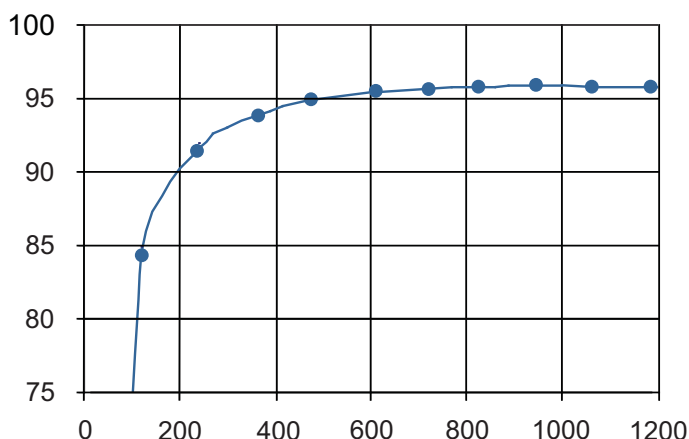
1. Connect Input voltage measurement leads to TP01 and TP02, on the Evaluation Baseboard. Observe correct polarity as marked.
2. Connect Output voltage measurement leads to TP04 and TP05, on the Evaluation Baseboard. Observe correct polarity as marked.
3. Insert a calibrated shunt in series with the –IN connection. The shunt should be capable of measuring up to 5 A of current.
4. Insert a calibrated shunt in series with the –OUT connection. This shunt should be capable of measuring up to 120 A of current.
5. Power the unit on.

6. Enable the unit using the array enable / disable switch.
7. Choose an appropriate temperature for taking the efficiency data and allow the unit to equilibrate to that temperature. If necessary, run the unit with some load to increase the rate of temperature rise.
8. Once equilibrated, set the load to the appropriate value and enable the unit. Take input voltage, current, output voltage, and current measurements and disable.
9. Repeat steps 6 and 7 for the desired range of load values.
10. Determine the efficiency (in. %) per the equation below:

$$\text{Efficiency} = \frac{\text{Vout} \cdot \text{Iout}}{\text{Vin} \cdot \text{Iin}} \cdot 100$$

Figure 12 shows efficiency data for a 0 – 1.2 kW load at 40°C case temperature with heat sinks.

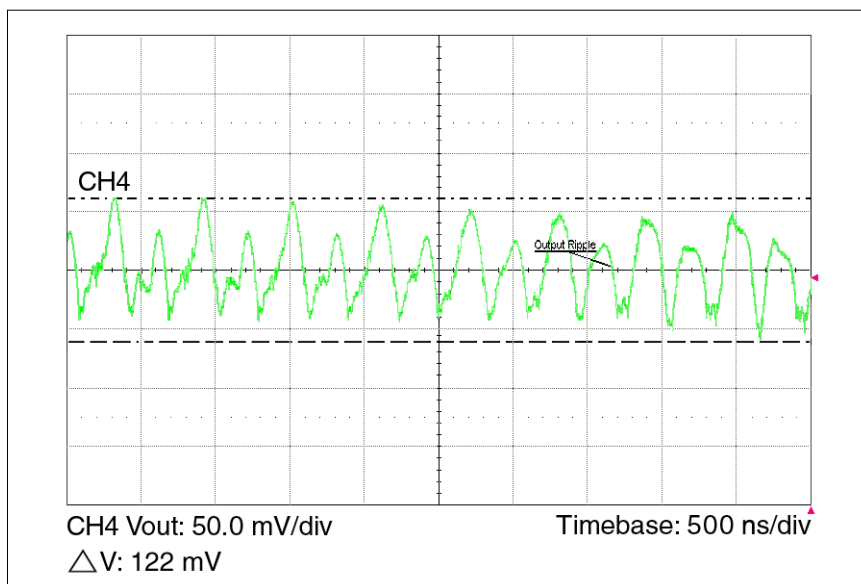
Figure 12
System efficiency



4.2 Output Voltage Ripple

J03 should be used for output voltage ripple measurements to minimize inductive noise pickup. To measure ripple, insert the scope probe into J03, apply power to system, set the load, and trigger the oscilloscope on the ripple. The BCM switches at approximately 1.5 MHz. Due to the rectification of the internal sinusoidal oscillator, the output voltage ripple appears at twice the switching frequency, approximately 3 MHz. Please see Figure 13.

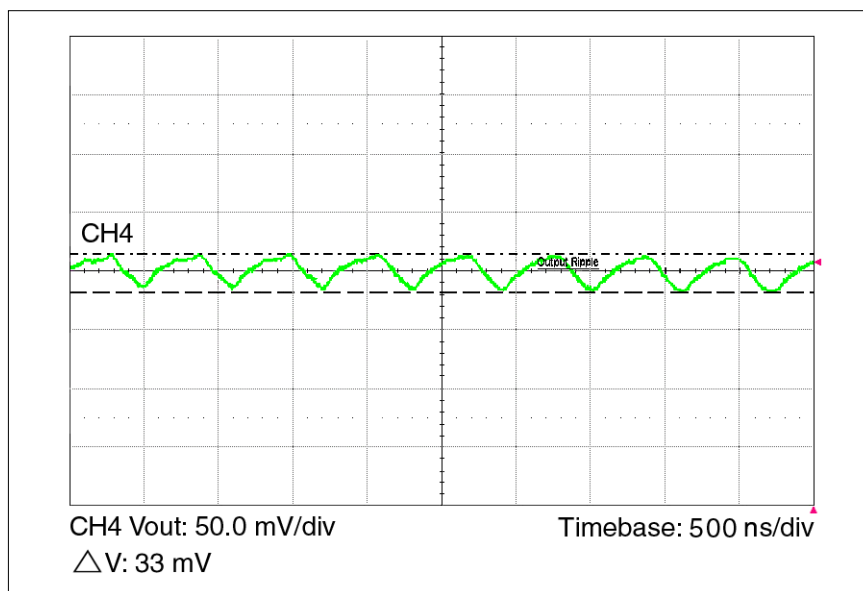
Figure 13
Output Voltage Ripple
at 100 A out



It is important to keep in mind that the BCM is an ideal voltage transformer at frequencies below 1 MHz and ripple voltage that appears on the input will appear on the output as well, reduced by the K factor. This is especially important in systems where the BCM array is powered off of a PFC front-end. The 120 Hz ripple component of the PFC front end will appear on the output of the BCM reduced by its K-factor (in this case, 1/32).

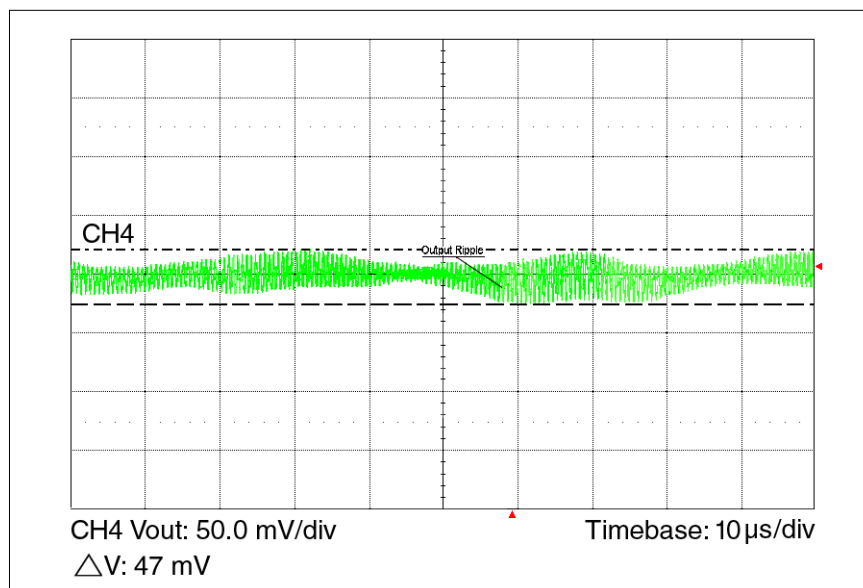
Ceramic capacitors can be added in positions C03 – C10 on the High Voltage BCM Parallel Array Evaluation Baseboard to reduce the output voltage ripple (Figure 14).

Figure 14
Output Voltage Ripple
at 100 A out with 80 μ F
ceramic output capacitance



Finally, given that this is an array of BCMs, each BCM switches at a slightly different frequency. The actual differences in switching frequency are minute, but will result in a low frequency beat attenuation that is visible on the output (Figure 15). This beat frequency is never greater than the ripple of a single BCM and is best attenuated with capacitance filtering.

Figure 15
Output Voltage Ripple
at 100 A out with 80 μ F
ceramic output capacitance,
showing beat frequencies



4.3 Enable / Disable Timing

Figure 16 and 17 illustrate the basic timing between output voltage rise and high PC, or application of input power.

Figure 16
Output Voltage rise time
on PC enable

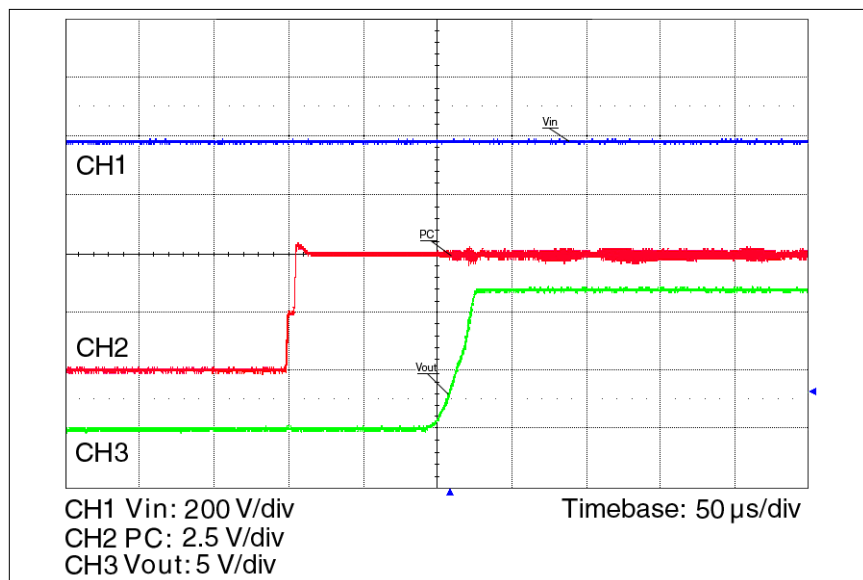
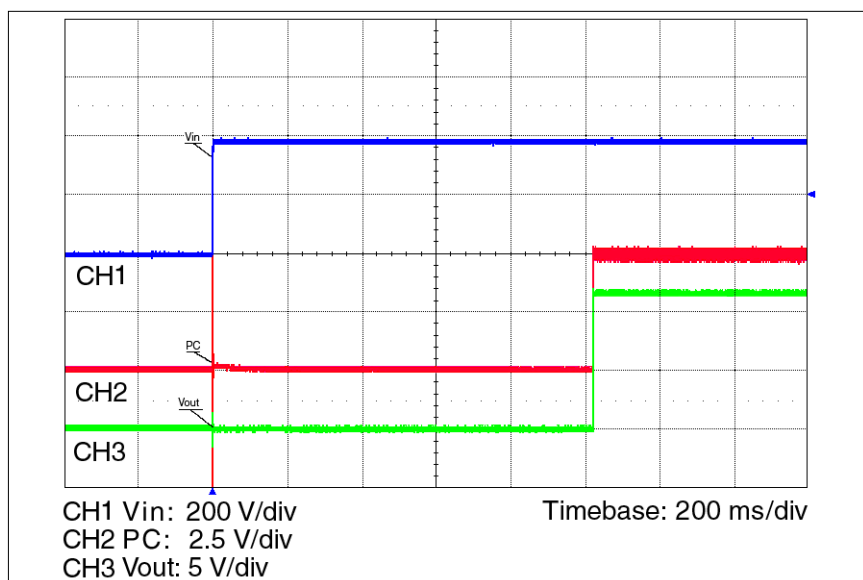


Figure 17
Output Voltage rise time
after application
of input power



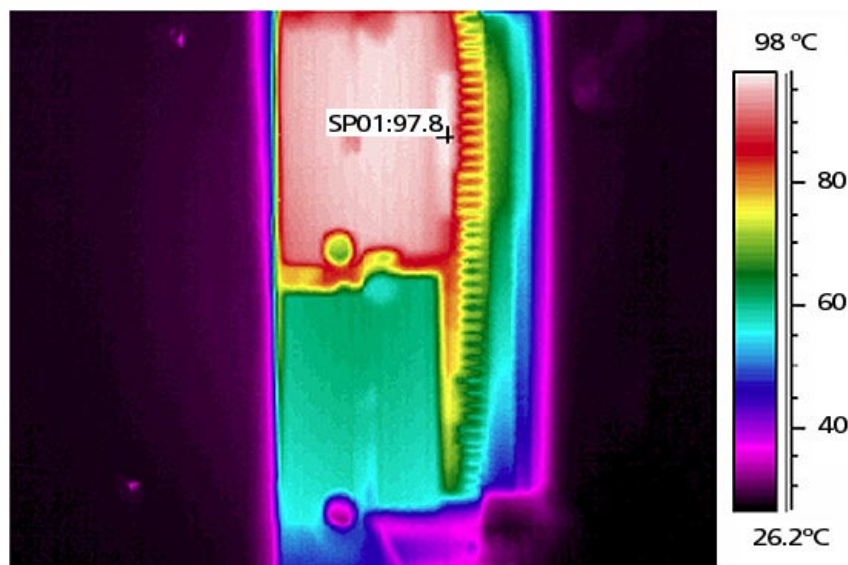
4.4 Thermal Testing

As with any high-density power system, it is important to design a robust thermal management system which adequately cools the system under all ambient conditions. The High Voltage BCM Parallel Array has high power density, but it also has a relatively high heat density. The BCMs dissipate approximately 15 W each at full load, and the interconnect losses are approximately 7-8 W at 100 A. This section will discuss some details of cooling a vertical mount product.

The BCM can be cooled via two paths, through the PCB, to ambient, or through the case to ambient. For more details on the thermal management of the BCM, please see [AN:008](#). The High Voltage BCM array does not enable any cooling through the PCB. This is due primarily to two factors 1) the double-sided construction of the system and 2) the lack of copper on the primary (high voltage) side of the board. Thus virtually all of the cooling must be done through the case.

Since the array has two BCMs inline, inline cooling will provide one BCM with the cool inlet air, and the second BCM with heated air from the first BCM. The end result is that one BCM may be substantially hotter than the other when employing inline cooling (Figure 18). Ways to equalize the temperature between BCMs include a) using different height heat sink or b) blowing air orthogonal to the array, or c) using a single heat sink to cool both V•I Chips on each side. In the latter case, both sides of the board must be cooled separately.

Figure 18
Inline cooling of BCM Array,
illustrating the temperature
difference between the first
and second V•I Chips
at 100 A, 25°C ambient,
with 400 lfm of airflow
(no ducting)



5.0 Conclusion

The High Voltage BCM Parallel Array system is ideal for evaluating the potential of using V•I Chips in post PFC or high voltage DC applications to power downstream regulators and niPOLs. If you require any additional assistance, or would like further design support, Vicor Applications Engineering is available to assist.

Technical advice furnished by Vicor is provided as a free service, with the intent to facilitate successful implementation of Vicor Products. Vicor assumes no obligation or liability for the advice given or results obtained. All such advice given and accepted is at user's risk.

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